CORROBORATIVE ANALYSIS OF NONVOLATILE MEMORY CHARACTERISTICS OF MEMRISTOR AND DESIGN OF A NEW DELAY ELEMENT

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Abstract- Next generation nano-computing extensively requires nonvolatile nano-scale memory devices for storage. "The missing fourth circuit element", Memristor is coming as a promising nano-scale applicant for nonvolatile memory design. This paper focuses on the study of basic Memristive equations, existence of the Memristive effect through modeling of a new nano device called Memristor and leveraging this to design a new delay element. Memristor is a two terminal passive element that relates the charge and flux. As its name suggest it is a memory resistor because of its property to remember the history. It offers the variable resistance whose value depends on the magnitude and the polarity of the applied voltage. Memristor holds the value of modified resistance even after withdrawal of applied voltage. These unique properties of Memristor differentiate it from existing passive elements i.e. Resistor, capacitor, and inductor and lead to numerous applications observing limitations from RLC circuits design. In this paper, nonvolatile memory property of Memristor is demonstrated, corroborated through simulation results and further it is extended in designing of a new delay element.

Keywords- Memristor; Memory Resistor; Non-Linear Modeling; Delay element.

I. INTRODUCTION

Recently, Memristor devices has made radical ingress in the field of VLSI design and added a new dimension for designing more efficient novel circuits and systems. Memristor is the fourth fundamental circuit element which was first conceptualized by L. O. Chua in 1971 [1] and after almost 40 years, Stanley Williams and his team in HP Labs practically realized a two-terminal titanium dioxide nano-scale device in 2008 [2-3]. Memristor is essentially a "Resistor with memory" provides many good features, such as high density, low-power, non-volatility, CMOS-compatibility, and shows great potential in data storage, logic computing, and artificial neural networks [4].

Memristors are basically the devices with varying resistance that depends on the charge that flows through it. When current flows in one direction the resistance of the device increases and contrary to it the resistance of the device decreases when current flows in opposite direction. When this voltage is turned off, the Memristor remembers its most recent resistance until the next time it is turned on. It means that Memristor memorizes the current that last flowed through it. Therefore Memristors can be used for memory implementation, where the logic bits are stored as resistance states [4, 9]. This refers to Non-Volatile RAM (NVRAM). This paper presents the logical analysis of the Memristor theory and the first bipolar Memristor developed at HP labs using PSPICE.

Delay locked loops, Phase locked loops, Asynchronous designs and complex mathematical circuitry all extensively consumes delay elements. The delay element produces the similar waveform in output as was applied at input with a predefined delay. Therefore design of a power efficient and true voltage controlled delay element is critical VLSI requirement [11]. Since the resistance of the Memristor can be controlled through the direction and amplitude of the voltage applied and this property is leveraged to design a voltage controlled delay element. The advantage of the Memristor delay element over other existing delay circuits is that the amount of delay can be programmed by simply varying the control voltage of the Memristor whereas in CMOS-based delay element W/L ratio has to be changed to get a new delay value[12-13]. Other benefits associated with this nano-device such as area and power efficiency are the added advantages.

The paper is organized as follows. Section II gives brief introduction to the basic Memristive device equations, properties of Memristor and its physical model. Section III describes the experimental circuit to simulate its nonvolatile memory characteristic. Also the design of a voltage controlled delay element circuit is presented here. Simulation results are presented and comparative analysis is explained in section IV. Section V concludes the paper.

II. MEMRISTOR AND ITS PHYSICAL MODEL

2.1. Memristor

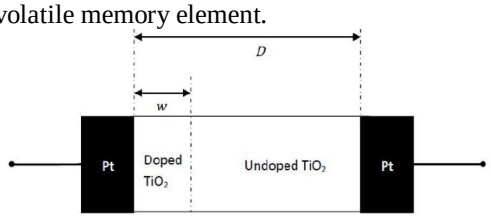
L. O. Chua hypothesized mathematically fourth passive element called Memristor as

$$d\varphi = Mdq \qquad (1)$$

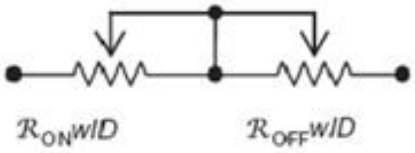
The Memristor can be defined in terms of a non-linear functional relationship between the flux linkage $\varphi(t)$ and the amount of electric charge that has flowed

through the device , q(t) [1]. Memristor is expressed as charge controlled or flux controlled depending on the expression as a charge controlled (q) or flux controlled (φ) function.

In 2007, R. Stanley Williams of Hewlett Packard confirmed that a solid-state device could have the characteristics of a Memristor based on the behavior of nano-scale thin films [2-3]. The HP Memristive device is composed of oxygen depleted thin titanium dioxide film sandwiched between two thick platinum electrodes. The depleted layer has a much lower resistance than the non-depleted layer as the oxygen vacancies act as charge carriers. The operation of the Memristor depends on the fact that the oxygen vacancies have the tendency to drift within TiO_2 with an applied electric field [5]. When an electric current is passed in a given direction the boundary between the high-resistance and low-resistance layer moves in the same direction. This change in resistance is reversible by changing the direction of current [7]. Since the oxygen vacancies have a low mobility, the oxygen ions do not migrate and they tend to stay in the same position when voltage is turned off. This property indicates that the device can be used as a non-volatile memory element.



(a)



(b)

Fig 1(a) Physical model of a Memristor (Schematic of HP Labs Memristor) [4], (b) Electrical structure of Memristor [7]

Fig. 1 (a) shows the basic model of a Memristor where D is the length of the device and w is the doped region length. Therefore the resistance of the device is low when w = D and is represented by R_{on} and for w = 0 the device offers very high resistance denoted by R_{off} shown in Fig.1 (b).

Thus the equivalent resistance of the device is the sum of the resistance of the doped and undoped layers. The V-I characteristics for the simplest case of ohmic conduction and the linear ionic drift in a uniform electric field can be written as

$$v(t) = \left(R_{on} \frac{w(t)}{D} + R_{off}\left(1 - \frac{w(t)}{D}\right)\right) i(t) \qquad (2)$$

where w(t) is the state variable represents the sharp boundary between the two layers. It is bounded between the limits 0 and D, corresponding to the position of the metal contact at either side of the TiO_2 film.

The Memristance can be expressed as,

$$M(q) = R_{off}\left(1 - \frac{\mu_v R_{on}}{D^2} q(t)\right) \qquad (3)$$

q(t), denotes the charge passed through the Memristor.

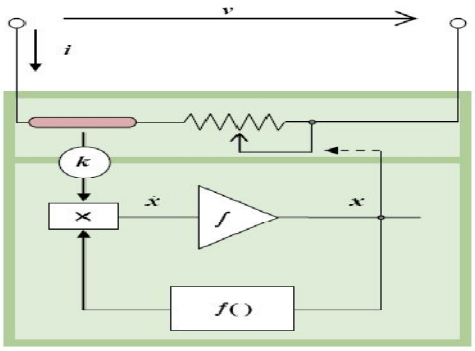


Fig.2: Block diagram of the Memristor Model [7]

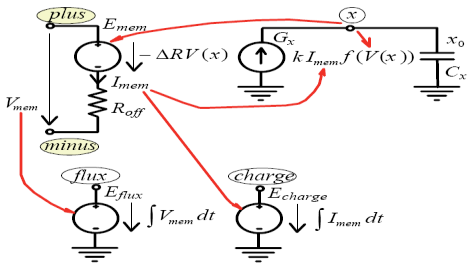


Fig. 3: Structure of SPICE model [7]

Based on these equations Memristor can be modeled by the block diagram in fig. 2. The Feedback-controlled integrator models the memory effect of Memristor. The passing current is stored through the integrator and through modifying the limiting boundary conditions the Memristance can be controlled. The nonlinear drift and the influence of the boundary conditions are modeled by the feedback via the nonlinear window function f(x) [5].

The circuit layout for a SPICE model [5] is shown in Fig. 3. The model is implemented as a SPICE sub circuit with parameters: the initial resistance, and resistances, the width of the thin film D, the dopant mobility μv, and the exponent p of the window function.

2.2. Hysteresis loop Characteristics

Since there is an integral relationship between the resistance of the Memristor and the current flowing through it forms the basis of the I-V characteristics to have a pinched hysteresis loop, revealing that the device has the memory effect associated with it. Fig. 4 shows the behavior of Memristor at different frequencies through V-I characteristics. Though the shape of the loop varies for different devices, but it always passes through the origin and is dependent on

the input voltage. For high input frequencies the device behaves as a linear resistor. It is clear from the curve that the device does not display hysteresis unless the voltage across the Memristor exceeds a threshold value. This proves the memory in passivity criterion. The area of the curve gives the charge passed through it. In this paper PSPICE analysis is carried out to verify the Memristive effect and is given in next section.

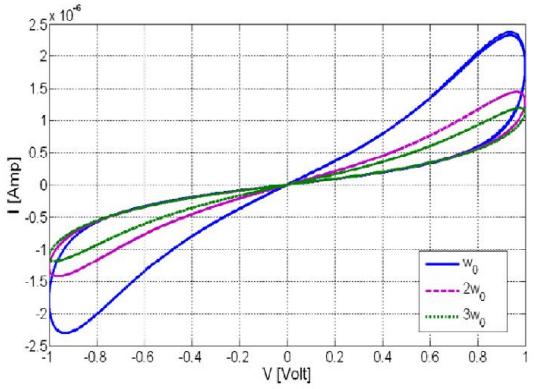


Fig. 4: V-I curve of Memristor showing Hysteresis loop

III. MEMRISTOR CIRCUITS

3.1 Memristive Characteristic

To verify the Memristive properties, it is analyzed using the circuit shown in Fig. 6 in PSPICE. Memristor is simulated using the model [5]. The values assumed in the model for Ron = 1k, Roff = 100k and the initial resistance Rinit = 10k. By varying the input voltage different resistance properties can be extracted out through this circuit.

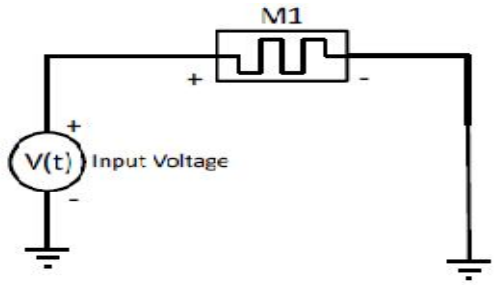


Fig 6: Circuit used to carry out the simulation (M1 is the Memristor and V(t) is applied voltage)

3.2 Voltage Controlled Delay Element

The property to remember different resistance value makes the Memristor apt for providing programmable delay in digital circuits. A delay circuit produces the same waveform as applied at its input only after a fixed value of time. There exist a number of delay elements proposed in previous works having different trade off and suits application accordingly [11-13]. In this paper a new voltage controlled delay element is designed using Memristor. This offers the advantage of less area, low power consumption and easily programmable delay. The circuit for the voltage controlled delay element is shown in fig. 5.

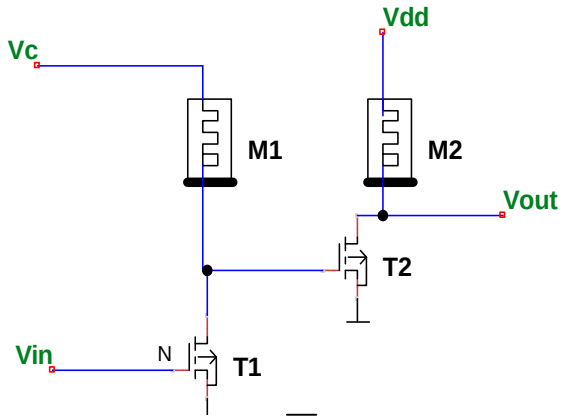


Fig. 5: Memristor-based voltage controlled delay element(M1,M2 are the Memristor and T1,T2 are the NMOS devices)

The circuit is composed of cascaded inverter pair with the controlling voltage, Vc, applied at the input of the Memristor (M1). By varying the value of the Vc the delay of this circuit can be varied accordingly. The delay depends on the value of Memristance by which it is programmed depending on the value of applied controlling voltage. Thus it is clear that the same circuit can provide different amount of delay by simply varying Vc. A square pulse is given to study the rising and falling transition to get the delay value. Delay t_p is calculated from the input-output waveforms and is given as the average of the time difference between input and output reaching 50% of V_{DD} for rise and fall transitions i.e. t_{plh} and t_{phl} respectively.

$$tp = \frac{1}{2}(tplh + tphl) \qquad (4)$$

IV. SIMULATION AND ANALYSIS

4.1 Memristive Characteristics Analysis

To get the V-I characteristics, a continuous periodic input is applied and a hysteresis loop is obtained. It can be seen from V-I curve that the resistance varies continuously and attains an extreme point as the applied current sweeps to either end. It can also be observed that the curve passes through the origin and also confirms the passivity criterion which tells that Memristor is a passive element if the incremental Memristor M(q)≥0.

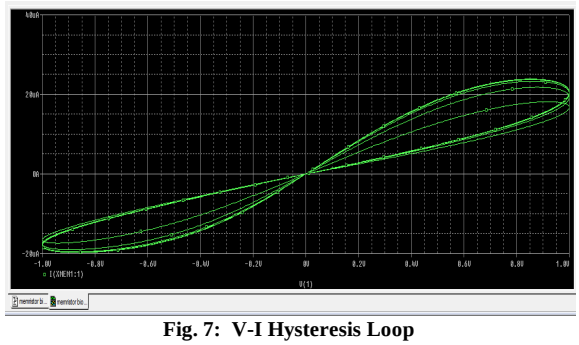


Fig. 7: V-I Hysteresis Loop

To corroborate the memory behavior of Memristor, a single input pulse is applied to the circuit. According

to the Chua's concept, the Memristor must program to certain resistance depending on the strength of the applied input and the time duration it is applied for. As soon as the pulse goes low the resistance in the device must lock to that value that depends on its previous state. The same has been verified by applying input voltage of different strength. It is seen that every time the Memristor remembers a different value of resistance depending on input voltage. This is given in series of graphs of Fig.8

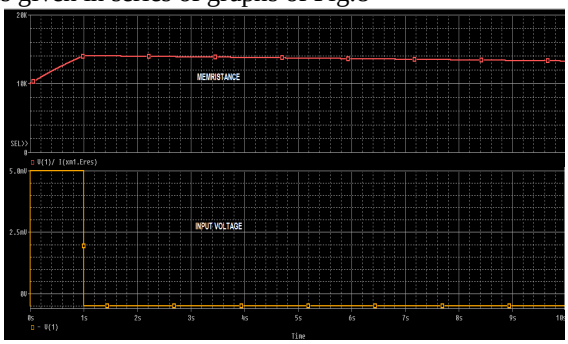


Fig. 8(a) :Small voltage of 5mv set the Memristance close to R_{init}

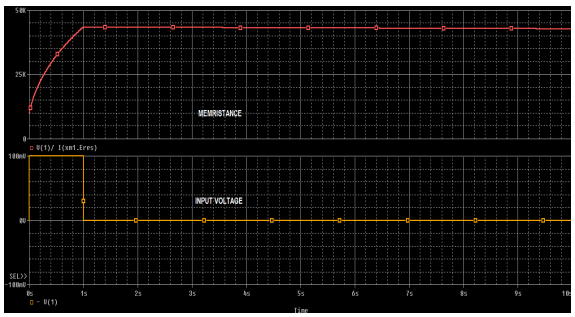


Fig. 8(b) :Voltage of 100mv set the Memristance just higher than R_{init}

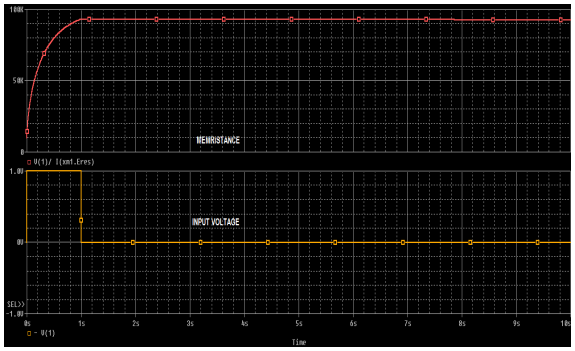


Fig.8(c): Voltage of 1v set the Memristance close to R_{off}

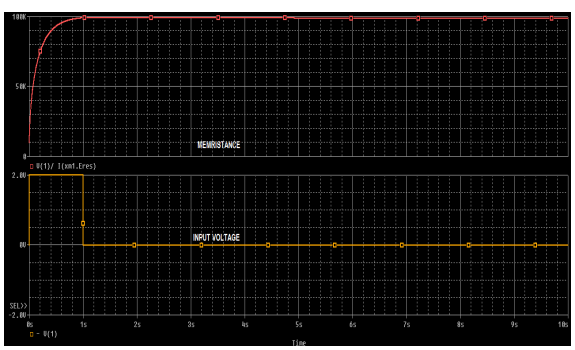


Fig. 8(d): Voltage of 2v set the Memristance equal to R_{off}

The above simulation result conforms to Memristance versus charge map as postulated in theory. From the above waveforms it is clear that the resistance transition depends on the integration of the current passing through it.

4.2. Voltage Controlled Delay Element

The proposed delay element in fig. 5 is designed and simulated on 1.2µm technology in PSPICE. The parameters passed to the Memristor model to carry out the simulation are: Ron = 1k, Roff = 100k and Rinit = 80k. Propogation delay and power consumption is measured for performance analysis of proposed delay element. The control voltage is varied in step and each value of propagation delay and power is measured. Fig. 9 describes the relation between the controlling voltage and delay, whereas the behavior of power consumption to delay is shown in Fig. 10. The performance comparison with the CMOS-based voltage controlled delay element given in [12] is produced in table 1. The results obtained are in accordance with the analysis. From the [12] the CMOS based delay element provides a variable delay range but at the cost of slightly higher area and power consumption when compared to the simple cascade inverters. This tradeoff in performance is catered in proposed delay element and is substantiated from the table.

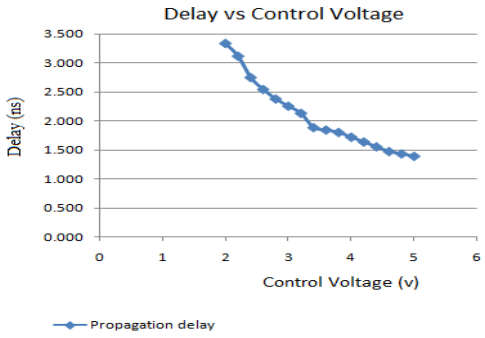


Fig 9: Delay vs Control voltage graph

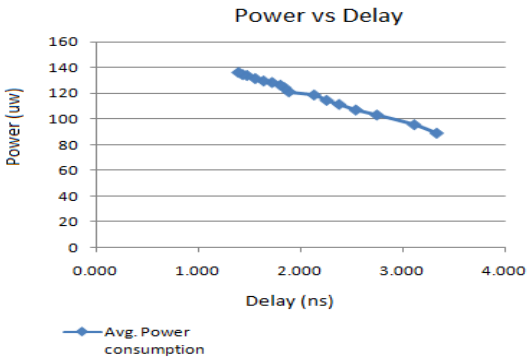


Fig 10: Power vs Delay graph

Table 1 : Comparison of delay elements

Delay Element(Voltage Controlled)	Delay (ns)	Power Consumption (uw)
CMOS-based	1 – 3	230 – 310
Memristor-based	1.4 - 3.33	88 – 136

CONCLUSIONS

In this paper the Memristor characteristics has been analyzed using PSPICE and found that the results are in accordance to the theory given by L.O. Chua. Further the first physical model developed by HP labs has been described. The voltage controlled resistance property of Memristor is leveraged to design a novel delay element and simulation results are found in accordance to the design analysis. The delay element has the true voltage controlled delay range of 1.4 to 3.3 ns, relatively lesser power consumption and due to nano-scale dimension better area efficiency as well. Due to its nano-scale dimension and pinched hysteresis the Memristor may be a potential applicant for the design of Memory system and computer architecture.

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