CIRCUIT DESIGN AND IMPLEMENTATION OF HYSTERESIS CONTROLLED BOOST CONVERTER

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Abstract- In this paper, we achieved hysteresis controlled boost converter. We used the architecture of the charge pump with hysteresis comparator for low output ripple to achieve boost convert purpose. The characteristic of hysteresis comparator is to efficiently decrease output ripple, at the same time limit output ripple about 50 mV to 55 mV. Under circumstances of output load adjust, will still provide fine transient response performance. The peak efficiency is 81.95 % and the power consumption is 14.46 mW. We used TSMC 0.18 µm CMOS 1P6M process for HSPICE simulation and finished the work of tape out service. This design in the post-layout simulation with HSPICE under different variation of environment, the simulation results show that this circuit is functioning properly. The chip area is 0.723 mm x 0.723 mm.

Keywords- Hysteresis, Voltage Booster, Peak Efficiency, Voltage Converter.

I. INTRODUCTION

In order to increase the convenience of life, different functions of electronic products are out with the old. Electronic products such as mobile phones, cameras, tablet PCs and other devices are composed of many integrated circuits and different type of integrated circuits require different power supply. In the case of fixed power supply, we need boost converter to change bias voltage for using of different chips. With the technology of changing and market demand, electronic products tend the development of thinness, lightness, convenience and multifunctional; therefore, with the situation of more multifunctional electronic products, the boost converting and controlling is more important. As mentioned above, in the case of more advanced process technology and much thinner and lighter electronic products, the circuit with providing accurate boost converting is an important issue.

Charge pump is a switch mode converter [1][2]. It could be used to provide voltages higher than bias power or voltages of opposite polarity. These charge pumps could provide several times of voltage than power supply. The most famous is Dickson charge pump [3][4], using capacitors with diodes as switches for achieving charge pump. In order to improve Dickson charge pump, using transistors replace diodes as switches [5]. The designers could select different orders in series of capacitors and switches for achieving higher output voltage, that's why Dickson charge pump is the most famous.

The traditional switched capacitor converters were lossless and have no inductance to save chip size [6]. Lee proposed automatic pumping control scheme to realize converter in 2006 [7], composed of automatic pumping current control scheme and automatic pumping frequency control scheme. The former automatically adjust the size of pumping driver current to reduce output ripple. Kwan proposed digital-control dual-mode switched capacitor converter in 2013 [8], with light loading, the control loop operates in pulse-skipping mode (PSM), and with heavy loading, the control loop operates in frequency modulation mode (FMM).

Furthermore, the traditional inductor boost converter has excessive output ripples [9]-[11], and the larger the output load current the bigger the ripple is. This will produce a bad effect or malfunctions for the controller and the OP-sensor. In order to overcome the above drawbacks, Hwang proposed adaptive slope generator with hysteresis voltage comparison techniques in 2015 [12], successfully limited the maximum output ripple at 19.2 mV, and the peak efficiency is 90.99 %.

Most of the boost converter will be used charge pump as the part of power supply convert, with the subsequent circuit controls the output voltage after converting. The voltage after converting will deviate, which called output ripple, different loads cause different output ripple, when the output ripple is too large, the boost convert will not be accurate. In this paper, we focused on the output ripple to achieve the boost converter, we do not need high output voltage, so we only realized basic charge pump composed of capacitors and diodes. In order to achieve accurate boost convert, we used hysteresis comparator to realize hysteresis controlled boost converter (HCBC), analyzed and designed circuit for different loads.

II. HYSTERESIS CONTROLLED BOOST CONVERTER

The objective of the proposed hysteresis controlled boost converter is to convert the supply voltage of 1.8 V to an output voltage of 2.5 V. Fig. 1 shows the circuit diagram of the proposed HCBC which includes three portions: 1) the switch circuit; 2) the voltage booter; 3) the hysteresis comparator.

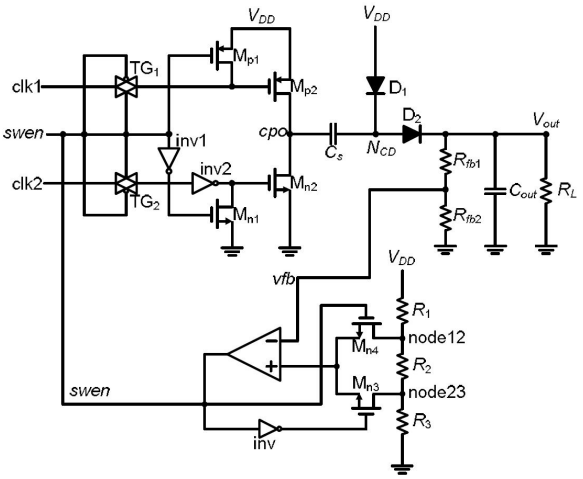


Fig. 1. Hysteresis contolled boost converter (HCBC).

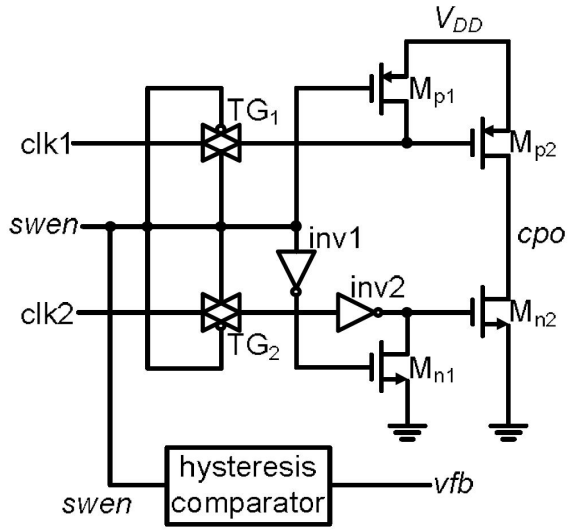


Fig. 2. Switch circuit.

A. Switch Circuit

Fig. 2 is the circuit diagram of the switch circuit. The function of this circuit is to receive the signal *swen* for controlling the operations of the succeeding voltage booster. This circuit is composed of two transmission gates, two inverters, two push-up transistors, and two pull-down transistors. The operations can be divided into two phases according to the signal of *swen*.

When the signal of *swen* is 0, the switch circuit will be disabled. The transmission gates will be turned off, and the clock signals *clk*1 and *clk*2 will be gated by the transmission gates. The transistors M_{p1} and M_{n1} will be turned on which will push up and pull down the gate voltages of the transistors M_{p2} and M_{n2} to V_{DD} and 0, respectively. Therefore, the node *cpo* will become floating.

On the other hands, when the signal of *swen* is V_{DD}, the switch circuit will be enabled. At the same time, the transmission gates will be turned on, and the clock signals *clk*1 and *clk*2 will pass the transmission gates to control the transistors M_{p2} and M_{n2} such that the voltage booster will operate normally.

B. Voltage Booster

Fig. 3 is the circuit diagram of the voltage booster. In the case of the signal of *swen* is V_{DD}, the switch circuit will be enabled. During this phase, the operations of this circuit can be divided into two modes: 1) setup mode and 2) pumping mode.

The circuit is operated in setup mode when the clock signals $(clk1, \overline{clk2}) = (V_{DD}, V_{DD})$. In this case, the transistor MP2 will be turned off while the transistor M_{n2} will be turned on. Therefore, the diode D_1 will be forward biased while the diode D_2 will be reverse biased. The capacitor C_s will be charged such that the node voltage $V_{N_{CD}}$ approaches 1.2 V which is lower than the supply voltage by 0.6 V because of the voltage drop across the forward-biased diode D_1.

On the other hand, the circuit is operated in pumping mode when the clock signals $(clk1, \overline{clk2}) = (0,0)$. In this case, the transistor M_{p2} will be turned on while the transistor M_{n2} will be turned off. Therefore, the diode D_1 will be reverse biased while the diode D_2 will be forward biased. The voltage at the node *cpo* will be pumped to V_{DD} (1.8 V), the node voltage of $V_{N_{CD}}$ will be pumped to 3 V, and the output voltage will be pumped to 2.4 V instead of 3 V because of the voltage drop of 0.6 V across the forward-biased diode D_2.

Consider the resistors R_{fb1} and R_{fb2} in the feedback network and the load resistance denoted as R_L at the output node. The output voltage V_{out} in setup mode and pumping mode can be expressed as

$$V_{out}(t) = \frac{\exp(Z/C_{out})}{C_{out}} \int \exp(Z/C_{out}) \cdot I_{C_s}(t) dt$$

and

$$V_{out}(t) = A\exp(Z/C_{out}\, t),$$

respectively. The constant Z can be expressed as

$$Z = \frac{R_{fb1} + R_{fb2} + R_L}{(R_{fb1} + R_{fb2})R_L},$$

and $I_{Cs}(t)$ stands for the current flowing through the capacitor C_s from left to right.

In the case of the signal of *swen* is 0, the switch circuit will be disabled. The output voltage will be discharged.

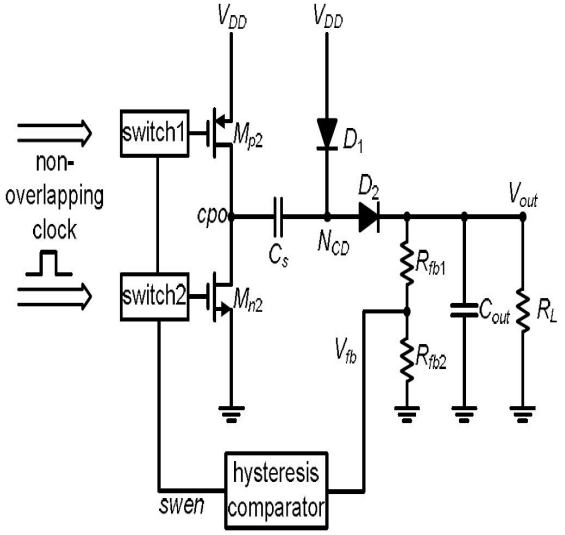


Fig. 3. Voltage booster.

C. Hysteresis Comparator

The objective of this circuit is to limit the ripple of the output voltages in a feasible range. Fig. 4 shows the circuit diagram of the hysteresis comparator. The resistors R_1, R_2, and R_3 construct a voltage divider which provides a voltage of 0.81 V at the node between R_1 and R_2. It also provides a voltage of 0.79 V at the node between R_2 and R_3. The signal *swen* controls the pass transistors M_{n3} and M_{n4} to set the reference voltages at the non-inverting terminal of the comparator to either 0.81 V or 0.79 V.

Initially, consider the voltage of *swen* is V_{DD}. The pass transistor M_{n4} will be turned on while the pass transistor M_{n3} will be turned off. The reference voltage of the comparator will be set to 0.81 V. In this case, the switch will be enabled, and the voltage booster will operate in setup mode and pumping mode alternately. Therefore, the output voltage V_{out} will be boosted in turn. The feedback resistors R_{fb1} and R_{fb2} are designed such that when the output voltage V_{out} exceeds 2.53 V, the feedback voltage V_{fb} will exceed 0.81 V. The signal of *swen* at the output of the comparator will transits to 0 V, and the reference voltage of the comparator will be set to 0.79 V. In this case, the switch circuit will be disabled, and the output voltage V_{out} of the voltage booster will be discharged. When the output voltage V_{out} is below 2.47 V, the feedback voltage V_{fb} will be lower than 0.79 V. The output voltage *swen* of the comparator will transits to V_{DD}, and the reference voltage of the comparator will be set to 0.81 V. Therefore, the switch circuit will be enabled again, and the voltage booster will alternatively operate in setup mode and pumping mode.

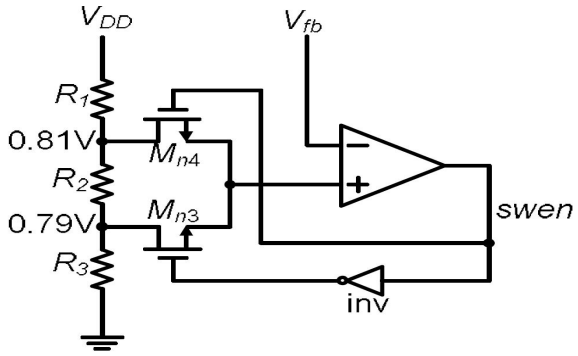


Fig. 4. Hysteresis comparator.

III. EXPERIMENTAL RESULTS

Simulations were carried out to verify the functionality, the power consumption, and the peak efficiency of the circuit as listed in Table 1. The proposed design is simulated using TSMC 0.18-micron CMOS process technology with HSPICE under nominal condition at a supply voltage of 1.8 V, 27 ºC. Figs. 5 and 6 are the physical layout and floor plan of this design, respectively. The chip area is 0.723 mm x 0.723 mm. For the generality, we consider different values for the load resistance at the output node. Fig. 7 shows the results of the post-layout simulations with the load resistances of 2 kΩ and 10 kΩ. The simulation results indicate that the proposed design is able to convert the input voltage of 1.8 V to an output voltage of 2.5 V well. The maximum output ripple is 54 mV. The power consumption is 14.46 mW. The peak efficiency is 81.95 %.

CONCLUSION

A hysteresis controlled converter is designed and implemented in this paper. The charge pump circuit associated with the hysteresis comparator efficiently decrease the output ripple which is limited in the range of 55 mV. Different resistances ranging from 2 kΩ to 10 kΩ were considered to simulate the variations in the output load. This design can convert the input voltage of 1.8 V to an output voltage of 2.5 V successfully. On the average, the power consumption is 14.46 mV under the supply voltage of 1.8 V. The peak efficiency is 81.95 %.

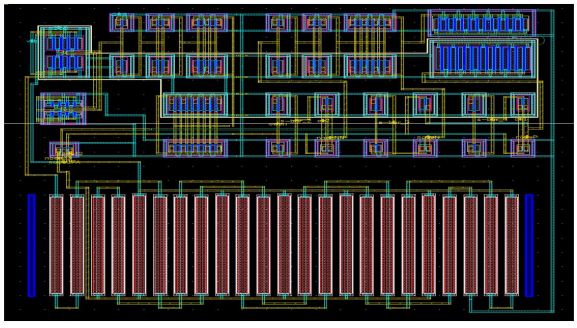


Fig. 5. Physical layout of the proposed HCBC.

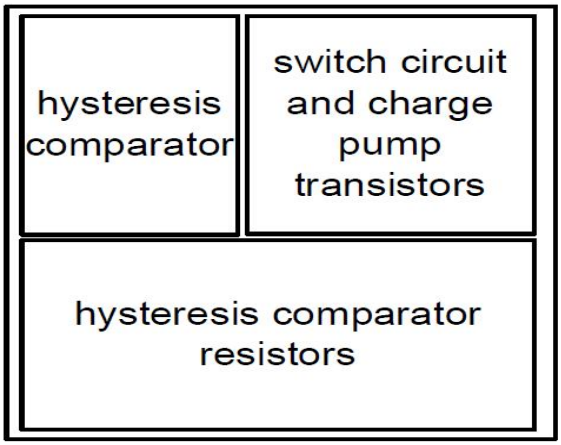


Fig. 6. Floorplane of the physical layout.

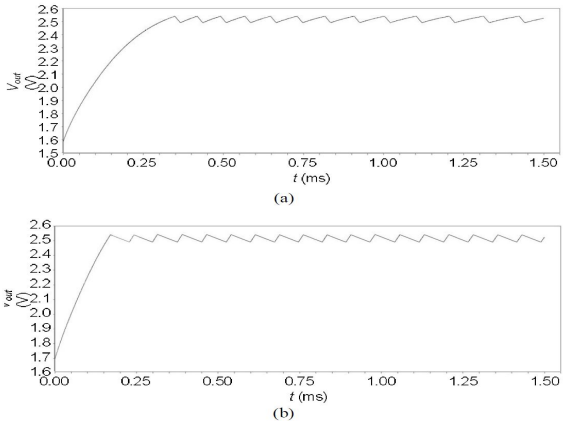


Fig. 7. Post-layout simulation results. (a) □ 2 k□ L R . (b) □10 k□ L R .

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TABLE 1 PERFORMANCE COMPARISONS

	[7]	[8]	[9]	[10]	[12]	This work
Technology (µm)	0.13	0.5	0.13	0.18	0.35	0.18
Topology	switched capacitor	switched capacitor	switched inductor	inductor based	switched capacitor with inductor	switched capacitor
Input voltage (V)	3.3	3.3	1.2-2	1.6-2	3.3	1.8
Output range (V)	4.5–5	1.8–5	3–5	2.5–4	3.6–5.1	2.5
Switching frequency (MHz)	0.4-0.6	5	100	100	1	1
Max. output ripple (mV)	33.8	125	N/A	200	19.2	54
Peak efficiency (%)	75	81.7	64	63	90.99	82

★★★