# DESIGN OF LOW COMPLEXITY CONSERVATIVE TESTABLE GATE USING QUANTUM-DOT CELLULAR AUTOMATA

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**Abstract:** Consideration faults and fault tolerance become important in physical realization of the circuits. In this paper, a new designofuniversal testable parity preserving QCA logic (t-QCA) is presented. Parity preserving circuits would be ideal for fault detection, since here the parity of the inputs is the same as the parity of the outputs. Hence, if there is a fault on any single output, the parity should be flipped which would make the fault easy to detect.The t-QCA is able to detect permanent and transient faults at the same time. The proposed design can be realized in error detection and correction circuits with significant improvements. The new design of t-QCA parity conservative gate is considerably declined in terms of cell numbers, occupied area and its delay is kept at minimum in comparison with the other previous circuits.

**Keywords**: Nanotechnology, Quantum-Dot Cellular Automata ,Fault Detection, TestableGate, Conservative Logic.

## I. INTRODUCTION

CMOS technology is not possible to decline feature size incomparably. It has some inconvenience such as high leakage current, high power consumption, circuit density and alsohigh lithography cost. Nanotechnology quantum-dot cellular automaton (QCA) is one of the emerging nano-technologies that can overcome these kinds of challenges [1].

Quantum dot is a region where an electron is quantum mechanically confined. A quantum cell consists of such quantum dots at each corner of a square and contains two free electrons. The electrons can quantum-mechanically tunnel among the dots and settle either in polarization P = − 1 (logic 0) or in P =+ 1 (logic 1). There are two different polarizations shown in **Fig.1.** Further, unlike conventional logic circuit in which electric current transfers information, QCA utilizes the Coulombic interaction of the electrons to propagate the polarization effect from one cell to another. By placing QCA cells side-by-side a binary signal propagates from input to output because of the coulombic interactions between cells [2].3-input majority gate is an elemental pattern in QCA [3] that shown in **Fig.2.** It is possible to build up AND gate or OR gate with majority gate by fixing one of the three input cells -1 or +1, respectively.

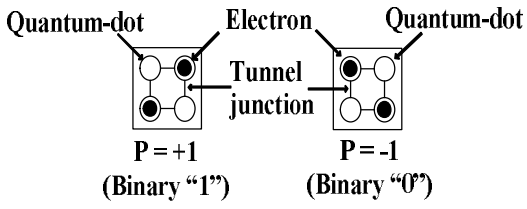



**Fig.1. QCA cells with two different polarizations.**

$$M(A,B,C) = AB + BC + AC; \textbf{(1).}$$

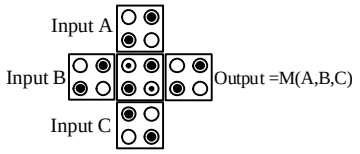



**Fig.2.QCA 3-input majority gate.**

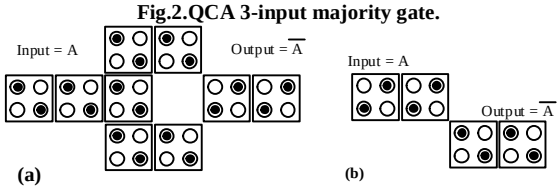



**Fig.3. QCA inverter structures a) robust inverter, b) simple inverter.**

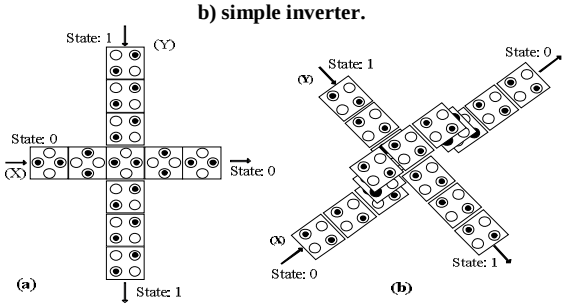



**Fig.4. Typical wire-crossing techniques a) coplanarcrossover with 45 and 90-degree wires, b) multilayer crossover.**

Inverter gates also the elemental pattern. Structures of inverter gate in QCA are shown in **Fig.3.**

Basically, there are two types of wire crossing multilayer and coplanar crossing, respectively. The coplanar and multilayer crossovers are as shown in **Fig.4.**

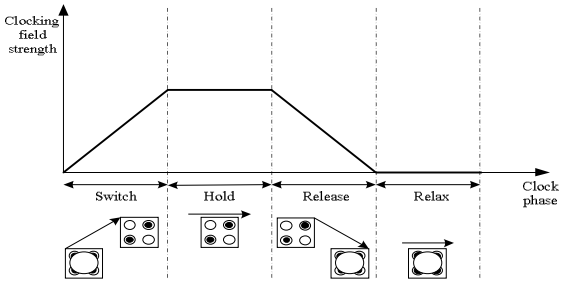



**Fig.5. Clocking scheme.**

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Clocking has implemented a transfer of electrons between the dots in QCA. QCA clocking monitoring data stream and provides with power to run the circuit. There is timing/synchronization mechanism in QCA that is implemented by the cascaded clocking of four distinct and periodic phases. These phases are Switch, Hold, Release and Relax as shown in **Fig.5** [4,19].

Generally, the synthesis and deposition phases happen defects in QCA circuits [5,17]. The deposition phase is sensitive to defects. In manufacturing phase QCA cells have not defects. Cell misplacement canoccur metal QCA faults. These defects named as cell misalignment, missing cell, cell displacement, rotation cell and additional cell [6,18].

Cell misalignment; with reverence neighboring cells force, defected cell is improperly lined up. After occurring cell misalignment, the defected cell gets closer to one or some cells faraway.Missing cell (cell omission); when a cell is missing compared to the original fault-free device Cell omission occurs. Cell displacement; if a cell is mislaid from its initial direction, cell displacement occurs. In this way, distances of the defected cell and all other cells are mutation either dwindle or increment. Rotation cell defect; a cell is displaced/rotated from its original position by an angle of θ. Additional (extra) cell; afterwards, an additional cell is inappropriately deposited on the substrate this defect occurs.

By parity checking techniques reduce the complexity of error detection and testing. The parity preserving logic gate; the parity of the inputs is the same as the parity of the outputs. If there is a fault on any single output, the parity should be flipped which would make the fault easy to detect [7,20].

## II. RELATED WORK

Including the evolution of new technology, also the deliberation of faults and fault tolerance became important. It has been suggested that parity preserving circuits would be ideal for fault detection, since here the parity of the inputs is the same as the parity of the outputs [8,14,15,16]. Hence, researchers work which ambition to design testable logic employ conservative logic and parity preserving logic.

There are several an existing popular conservative gates, such as Fredkin [8], CQCA [9], MX-QCA [10] and t-QCA [11]. Among them, Fredkin gate which is a 3x3 gate is used extensively. It has three input cells and by the rule, the same amount outputs as shown in **Fig.6(a).** The outputs of Fredkin gate are $P = A$, $Q = \overline{A}B + AC$, $R = AB + \overline{A}C$. It is one of the parity preserving and universal gates. Fredkin gates main detriment is by this gate very problematic to create an enormous circuit [8,13].

Nevertheless, after produce CQCA and MX-QCA gates this problem is overcoming. The CQCA can be performed using only two majority gates and utilizes two clock zones whereas MX-QCA demands four clocking zones and five majority gates. The structure of CQCA and MX-QCA are shown in **Fig.6 (b)**and**Fig.6(c),** respectively. These gates are better than the Fredkin gate in terms of complexity, speed and area. The last suggested is t-QCA conservation gate that shown in **Fig.6 (d)**.The t-QCA has been enhancement over preceding gates. The block diagrams and QCA design of t-QCA-I and t-QCA-II are shown in **Fig.7 (a)** and **(b),** respectively.

The first example of t-QCA-I is single-layered coplanar implementation using three 3-input majority gates and three inverter gates. This structure is composed of 113 cells and it is occupied 0.12 $\mu m^2$ total area. t-QCA-II is also the single layered coplanar implementation using one 5-input majority gate, one 3-input majority gate and three inverter gates. It is conceptually a little different, because of 5-input majority gate. However, number of used cells is not decreased, conversely increased and equal to 116 cells. Occupation area of the design is approximately 0.11$\mu m^2$. In both two designs, the desired output is generated after four clock phases. Testing and analyzing is conducted in these to designs using QCADesigner tool and some missing cells are detected in both two layouts.

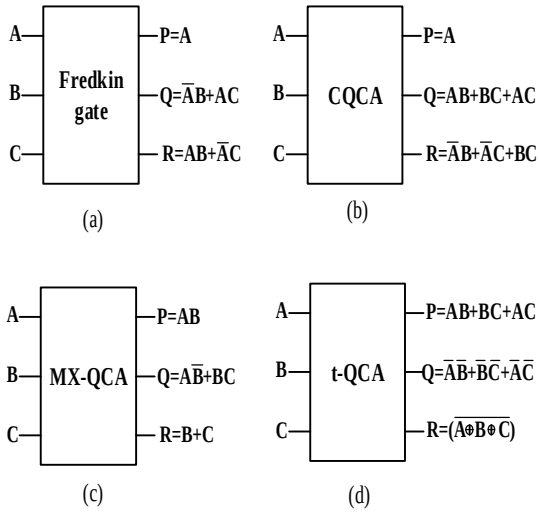



**Fig.6. QCA parity preserving gates a) Fredkin gate, b) CQCA gate, c) MX-QCA gate, d) t-QCA gate**

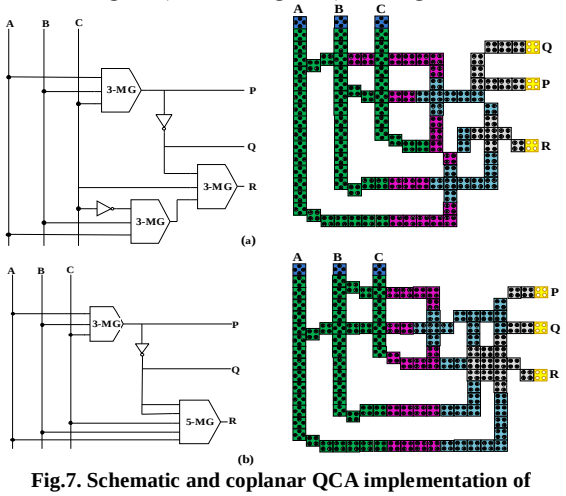



**Fig.7. Schematic and coplanar QCA implementation of t-QCA. a) t-QCA-I, b) t-QCA-II.**

## III. PROPOSED STRUCTURE

In this section, a new design of t-QCA is presented. The mapping of t-QCA from input-to-output is: $P=AB+BC+CA$, $Q = \overline{AB} + \overline{BC} + \overline{AC}$, $R = \overline{(A \oplus B \oplus C)}$ where A, B, C are inputs and P, Q, R are the outputs. The truth table of t-QCA is shown in **Table 1**. It shows that it has the same number of 1's in the input as in the output. To make a circuit parity preserved, the XOR of inputs must be equal to that of the outputs. Using the truth table of the t-QCA circuit, the value of input parity (A⊕B⊕C) and the output parity (P⊕Q⊕R) are calculated. After computed, it is clearly that the XOR of inputs equal to outputs. In this way t-QCA gate is parity conservative.

The schematic and QCA implementation of proposed new design of t-QCA gate are illustrated in **Fig.9(a)** and **(b)**, respectively. The proposed design is constructed by two gates, such as one majority gate and one explicit interaction cell based XOR gate. Inversion operations are realized using two-cell inverters. The construction of this layout is more proper to design complex and big circuits, because input cells are designed with regular cells.These kind of factors can be useful in realization process of sequential circuits.

**Table 1: Truth table of t-QCA.**

| Input | | | Output | | |
|---|---|---|---|---|---|
| A | B | C | P | Q | R |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

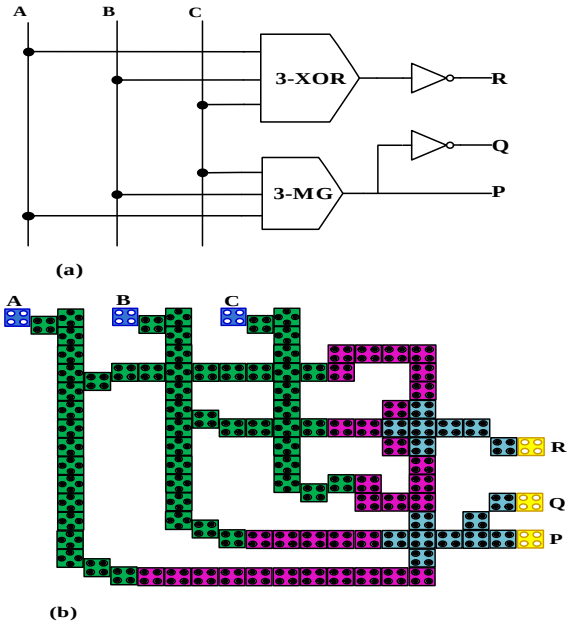



**Fig.9. New design of t-QCA implementation: a) Block diagram, b) QCA design.**

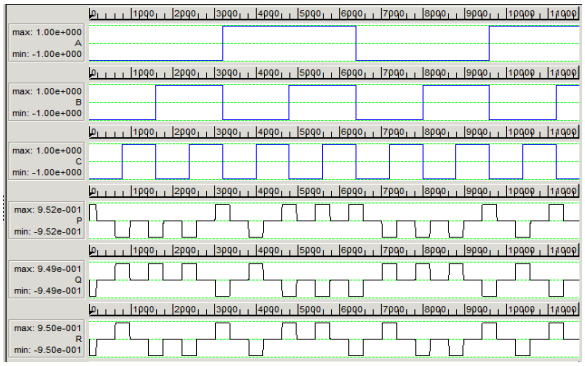


**Fig. 10. Simulation result of new design of t-QCA gate.**

## IV. COMPARISONAND ANALYSIS

The new design of t-QCA conservative gate is functionally simulated using the QCADesigner toolversion: 2.0.3 [12]. The simulation result of new design for t-QCA is illustrated in **Fig.10**. Analysis of the gained result confirms that the new design of t-QCA gate works well and expected result is achieved significantly. According to simulation result, the strength of the signal is stable and strong enough.

The comparison was done in terms of the majority gates (three-input and five-input majority gate) number of cells, clock phase and area of circuits. CQCA has better results in term clock zone. However,our proposal circuit has lowercomplexity than CQCA.As it can be seen from new design of t-QCA in-**Fig.9(b).**The number of clock phase is decreased. The output ofour circuit is produced after only 3 clock phases where as the one proposed in produces its output after 4 clock phase. Reducing clock zones is important, especially in large circuits. In term of cell count, our designneeds only 111 cells. By this, we get compact circuit which is smaller and dense thereby reducing wasted area.

| Conservative gates | MGs | | Cell count | Clock phase | Area ($\mu m^2$) |
|---|---|---|---|---|---|
| | 3-input | 5-input | | | |
| Fredkin[8] | 6 | 0 | 246 | 5 | 0.37 |
| MX-QCA [9] | 5 | 0 | 218 | 4 | 0.35 |
| CQCA [10] | 2 | 0 | 117 | 2 | 0.11 |
| t-QCA-I [11] | 3 | 0 | 113 | 4 | 0.12 |
| t-QCA-II [11] | 1 | 1 | 116 | 4 | 0.11 |
| Proposed circuit t-QCA | 2 | 0 | 111 | 3 | 0.10 |

**Table 2: Comparison of t-QCA and existing conservative gates.**

## CONCLUSIONS

In this paper, we have proposed a new design of t-QCA with improvements in terms of used cell count, circuit total area and other aspects. A clock of proposed circuit, namely latency is decreased and we used only 3 clock phases. Our circuit is optimal to

connect to other larger circuits. In the comparison, proposed t-QCAdesign has beenfound thatbetter design than the existing other designs. The new designcan reducearea and delay.

## ACKNOWLEDGMENTS

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