STRUCTURAL MODELING OF INTELLIGENT TRAFFIC LIGHT CONTROLLER ON FPGA

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Abstract- The paper presents an adaptive traffic light controller customized to have user defined number of intersection lanes and counts of signals for various intersections. Conventional traffic systems can be installed for a non-dynamic number of intersections with fixed counts of signal durations and are typically microcontroller based. The proposed system prototype is implemented on FPGA which offers many advantages over microcontrollers such as fast speed, number of input/output ports and enhanced performance coupled with low cost than ASIC design. Typical TLCs are modeled using the finite state paradigm and rely heavily on software design flow. In this paper, the hardware design has been deployed using the structural style of VHDL programming and thus offers more robustness. The system has been successfully tested and implemented in hardware using Xilinx Cyclone III: EP3C10F256C6. The efficient design thus offers a dynamic way that allows the user to design a robust TLC and thus it breaks through the bottleneck of traditional traffic signal controller, and can accomplish the control in complicated and diversified traffic.

Index Terms- TLC, FSM, Structural VHDL, Xilinx, FPGA

I. INTRODUCTION

At road intersections traffic lights or traffic lamps or traffic signals are generally positioned so as to control the traffic flow[1]. It is an electronic system generally installed on an intersection so as to notify the safety related issues with the help of specific predefined colour system (usually red, yellow and green. Traffic light controller (TLC) has been implemented using ASICs, FPGAs and microcontrollers. Some of the advantages of FPGA over microcontroller includes the number of I/O ports, speed of processing and performance, all of which are extremely critical in the design of TLC. The cost also is an extremely important issue in design of TLC. The reduced cost[2,3] increasing the use of FPGAs (Field Programmable Gate Arrays) for verification and implementation of a proposed system.

This has introduced FPGAs as ideal replacement for ASICs (Application Specific Integrated Circuits)[4]. With the exponential increase in the number of vehicles, the problem of traffic congestion and transportation delay has increased. This demands the need for increased safety and efficiency of the overall system. This can be achieved by making improvisations in the signalling element itself, i.e. the traffic light controller(TLC). In this paper, a traffic light controller which can be customized for variable number of intersections and duration of green signal has been designed, simulated and implemented on Xilinx Cyclone III: EP3C10F256C6.TLC has been designed by M.F.M.Sabri et al. [6] but real time implementation has not been carried out and only the behavioural simulations are shown. Shwetank Singh et al[7] have designed an effective method for busy and randomized traffic flow. The desired results such as time saving is achieved using the proposed Adaptive Dynamic Traffic Light Controller proposed in [7].

The developed functionality matches the real time requirements but the proposed paper takes into consideration the variable number of intersections and increases the robustness of the system. Papers [8,9] describe a low cost improvised traffic light controller system and offer a dual mode thereby offering intelligent control of traffic lights for various intersections. In this paper, the section II describes FSM modelling and state diagram. Section III describes the proposed system. Section IV includes the proposed algorithm, Section V describes the implementation of the proposed design on Xilinx FPGA and the simulation, compilation results. Section VI includes conclusion and the future work.

II. FSM MODELING AND STATE DIAGRAM

The traffic light controller is a sequential circuit and is modelled as a finite state machine. The number of states is a function of the number of intersections chosen and hence variable. For the purpose of description, a state machine for preliminary case of four intersections is described. The working of the state machine is described as follows:

Each sate in the state diagram corresponds to a traffic intersection. The transition from one state to other is

dependent on the timer. When the state machine is in a particular state, first of all, the green light corresponding to a particular lane glows for the duration as predefined by the user. Afterwards, the yellow light for the corresponding intersection is turned on for a predefined specific duration. Till this time, the remaining lanes show red light. Once the timer counts down completely, the machine switches to the next state. The state diagram is as shown in Fig.1.

t_g and t_y correspond to duration of green light and yellow light respectively. When t_g, t_y are non-zero, green light is turned on for the particular intersection and red for all the remaining ones. When t_g is zero, t_y is non-zero, yellow light is switched on for the particular intersection and when both the timers reach zero, red light is switched on the particular intersection and the machine moves to next state and the same procedure is repeated for the next intersection.

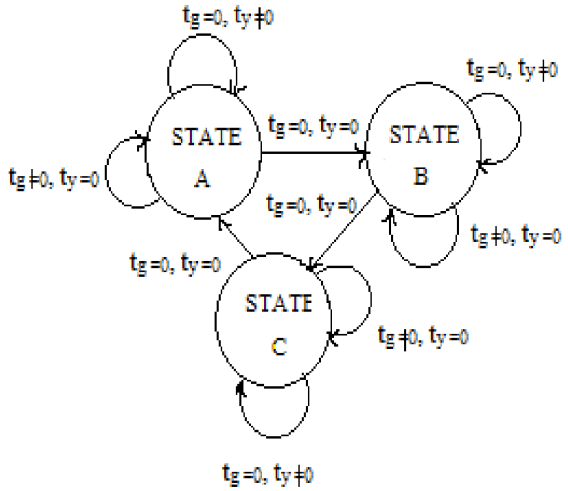


Fig. 1 FSM State Diagram

III. PROPOSED SYSTEM

The TLC is implemented on FPGA using the structural style of VHDL Programming. The flexibility of an FPGA benefits the design lifecycle, bringing savings in time and effort in the prototyping stage and in the integration of software and hardware in the design phase Majority of the conventional TLCS are modeled using the behavioral or data flow style of implementation using the method of nested iterations in finite state machine modeling. These methods fail in the case of occurrence of glitches as there is no way to troubleshoot the individual hardware components. For hardware realization of a robust TLC that functions 24x7 it is essential to have quick and efficient glitch reduction and troubleshooting methods. The structural style caters to all these cases and is thus used for design in the proposed algorithm. The design consists of various hardware components such as Input handing Units, Sequential circuits, Synchronizer, Timing Modules, Combinational Logic Circuits and Display Units.

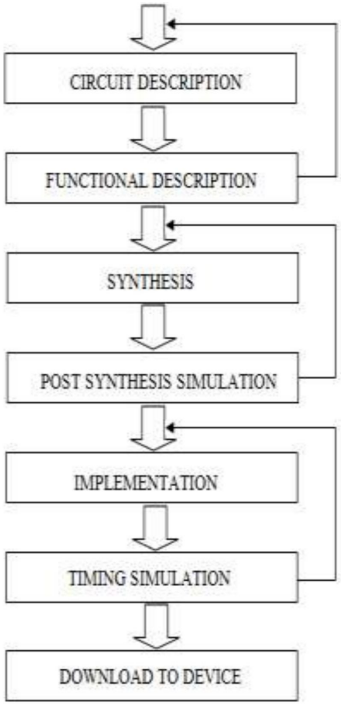


Fig. 2 Flowchart for Hardware Implementation

A. Input Handling Unit

The advantage of proposed TLC is customized inputs from the user for the number of lanes at intersections and count of Traffic Signal Duration. To achieve this the top level entity in the structural form design is the input handling mechanism. The user has the option to give variable intersections upto maximum of 7 and the count of duration for green signal from 0 to maximum of 100. The inputs can also be the outputs of various sensor networks used for motion detection. Typically, detection of moving vehicles is done by inductive loops, passive infrared sensors, magnetometers, microphones, radars or microwave sensors [9–12]. The inputs are fed to the sequential circuits and variable modulus counters which perform the further processing. The input entered by user is also presented on the display units for interactive user interface. There is also a universal mode key which decides the mode of operation of the entire system. There are two possible modes –day mode and night mode. The two modes are defined by the traffic density presence and thus govern the operation of the TLC 24x7. The timing module is next in line for the cascade of hardware components.

B. Timing Module and Synchronizer

This unit handles the master clock which governs the sequential operation of the various components in the design. The external display circuitry operates at 1sec to display the ongoing count of current intersection.

Thus the master clock at 50 MHz is down converted to operational frequency of 1Hz for the display units. The Synchronizer circuit governs this down conversion and operations of all system components at the required frequencies. In addition to synchronizing the input with the system clock, this process also ensures that the synchronized go signal is high for at most one clock period. In other words, this process ensures that the system behave correctly independent of how long the user presses the input push button.

C. Sequential Circuit

This consists of the variable modulus down counter with parallel loading facility. The input handling unit transmits the user values to this circuitry which then performs the required operation. The FSM modeling s implemented in the sequential circuit which produces the required variable duty cycle clock stream to produce the desired durations of the red , yellow and green signal light.

D. Display Unit

This circuit gives the display of the ongoing count in seconds on the 7 segment display unit, also the number of intersections selected and the mode of operation. The BCD convertors, decoders, multiplexers and the 7 segment display units are a part of this circuitry. The display unit provides an easy and efficient graphical user display of the current status of system operation.

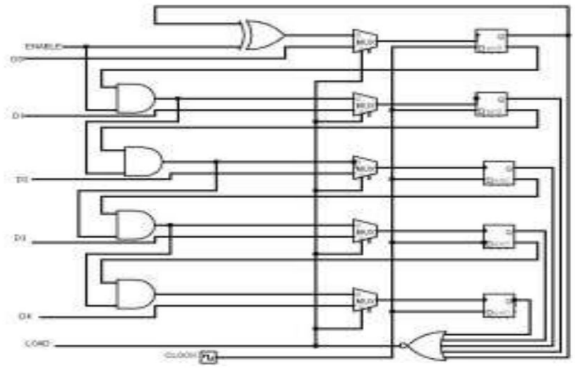


Fig. 3 Sequential Circuit Implementation

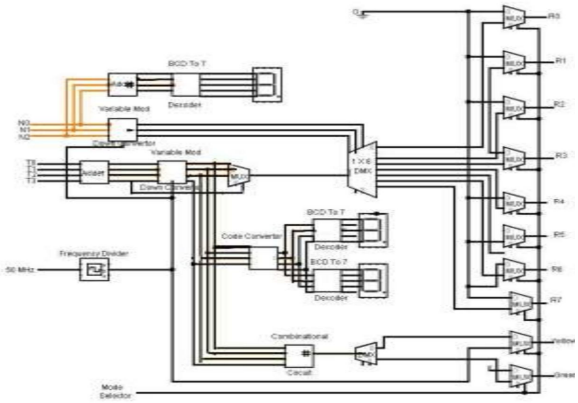


Fig. 4 Functional System Block Diagram

IV. PRACTICAL IMPLEMENTATION

The embedded platform used for implementation is the FPGAs (Field Programmable Gate Arrays), an early prototyping environment for a traditional ASIC (Application Specific Integrated Circuit).FPGA offers tremendous flexibility which brings savings in time and effort in the prototyping stage and in the integration of software and hardware in the design phase thereby benefitting the design life cycle. The design was implemented by synthesizing the VHDL structural code design, then generating a bit file using Xilinx ISE tools. This bit file was downloaded to the Altera development using Xilinx Cyclone III: EP3C10F256C6.

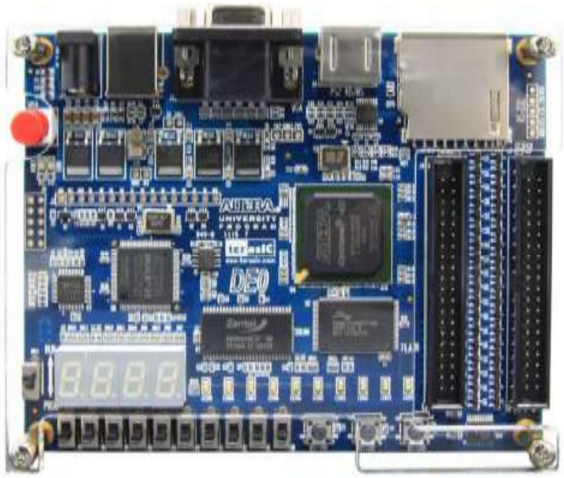


Fig. 5 Altera Development Board for FPGA

V. SIMULATION RESULTS

The VHDL test bench for all possible cases was simulated by using the ModelSim by Xilinx and the results offered complete success.

The design is robust for all user defined inputs for various input values and thus the proposed design performs as expected. The clock's display duration and graphical user interface is fully functional. It is capable of using all four digits of the seven-segment display and the board mounted am/pm LED indicator.

The reset switch works and the state machine does change state when the user presses the push buttons to change the mode of operation to day or night.

Thus the proposed system gives the realization of hardware system as well as the software system.

The experiment results show that the intelligent traffic control system can completely meet the requirements of modern traffic control and is robust enough to troubleshoot efficiently in urgent situations.

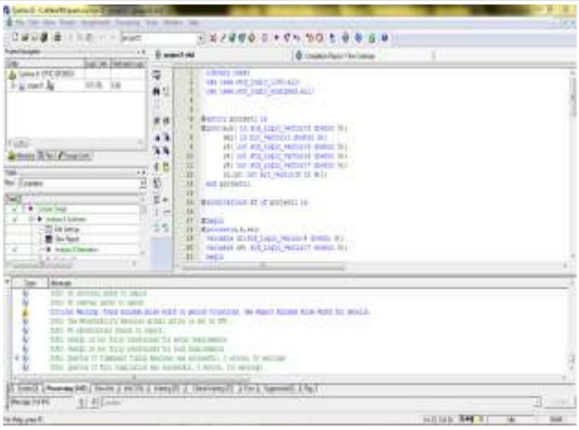


Fig. 6 Structural Modeling of System in VHDL

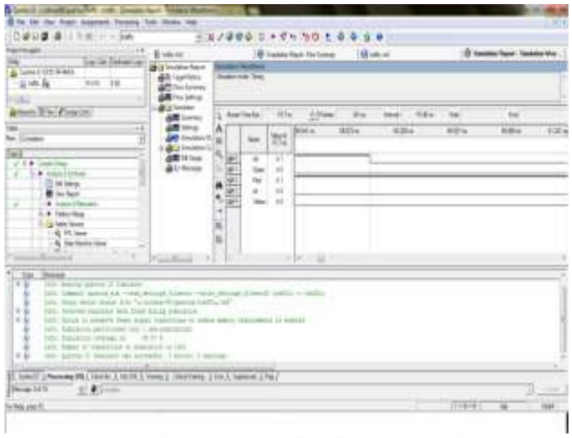


Fig. 7 Simulation Results for the Proposed Design



Fig. 8 Hardware Implementation on Xilinx FPGA

CONCLUSION AND FUTURE WORK:

All features needed for most complex designs have been offered in FPGAs. On-Chip Phase Locked Loop (PLL) or Delay Locked Loop (DLL) circuitry is used for clock requirement. In the proposed paper, the traffic light controller having customized settings for selection of the number of intersections and the duration of green signal has been designed. Simulation has been carried out on Quartus II Version 9.0. The timing analysis of the system provides cost effective and optimum results. The design flow is in structural style of modelling and hence the timing analysis of each and every component carried out and individually every component is tested on FPGA. This reduces the vulnerability of the system to glitches. The system has also been tested for all sets of possible inputs thereby avoiding any kind of hazard. The design has been implemented on FPGA(Specs to be added). The proposed design also qualifies for other performance metrics such as variable intersection capacity, safety, plus offers flexibility to choose and change the configuration of the system. Thus making it robust and generic. Future scope of this paper includes the use of neuro-fuzzy or image processing techniques in order to determine the real time traffic so as to provide a greater control over congestion.

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