ANALYZING ESD RELIABILITY STRENGTHENING OF 40-V NLDMOS WITH DRAIN-SIDE PARASITIC SCRS

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Abstract - This paper evaluated the effects of current path variation on the electrostatic discharge (ESD) robustness of n-channel lateral diffused MOSFET (nLDMOS) devices with drain side modulation fabricated in a 0.18 μm 40 V process. Through transmission-line-pulsing measurement, the secondary breakdown current (I_{t2}) of an nLDMOS with a drain side embedded silicon-controlled rectifier (SCR) structure and a pnp arrangement (DUT-2) was determined to increase from 2.498 A to >7 A (enhancement of at least 180%), compared with the reference nLDMOS device. The trigger voltage (V_{t1}) also decreased; in particular, the SCR (DUT-3) had the lowest reduction in V_{t1}. Moreover, the R_{on} value of the pure LDMOS (DUT-4) increased, and the I_{t2} value also increased from 2.498 A to 3.043 A (approximately 21.8% improvement). The results show that the I_{t2} (ESD immunity) value of the reference nLDMOS was lower than those of the pure SCR and pure nLDMOS constituting the nLDMOS-SCR (pnp arrangement); therefore, the I_{t2} value of the composite nLDMOS-SCR (pnp) device was higher than that of the reference nLDMOS.

Keywords - Electrostatic discharge (ESD), Holding voltage (V_h), n-channel lateral-diffused MOSFET (nLDMOS), Secondary breakdown current (I_{t2}), Silicon-controlled rectifier (SCR), Trigger voltage (V_{t1}).

I. INTRODUCTION

With the progression of semiconductor manufacturing technologies and miniaturization of devices, MOSFET devices have become thinner and junctions are shallower. These process characteristics reduce the electrostatic discharge (ESD) robustness of devices [1]–[5]. Therefore, developing an excellent ESD protection design to enhance the reliability of electronic products is critical [6]–[10]. An n-channel lateral diffused MOS (nLDMOS) could sustain a higher voltage [11]–[17], in addition to having a higher power density and being compatible with a low-voltage circuit. LDMOS power devices are commonly used as output drivers in smart power applications, and they are often used in input/output pads as self-protection units against ESD events. However, such high-voltage n-channel devices with a large number of fingers do not have high ESD immunity after entering the snapback conduction-on state. Such devices are prone to failure when operating in the snapback conduction-on state. This phenomenon is attributed to the current crowding effect among the multiple fingers, and this subsequently induces inhomogeneous triggering of the parasitic BJT, thus leading to a nonuniform turned-on state, which is problematic. However, because nLDMOS devices have a poor ESD capacity per unit area, they cannot effectively resist ESD bombardment. Embedding an SCR [18]–[28] in an nLDMOS device is a common method for strengthening device structures and reducing the trigger voltage, thus ensuring effective R_{on} conduction to protect the device against ESD damage. Nevertheless, some criteria must be met for the applications of nLDMOS protection devices in the high-voltage power era. Suitable triggering voltage (V_{tl}) and low on-resistance (R_{on}) values of the ESD device are required. Hence, the composite LDMOS-SCR is an efficacious solution for high-voltage ESD protection. The composite LDMOS-SCR has additional p^+ implants that are inserted into the drain end of an nLDMOS transistor to form an nLDMOS transistor coworked with an embedded parasitic SCR structure. The device integrates the desired behaviors of both LDMOSs and SCRs. The drift region of the LDMOS enhances the triggering voltage of the LDMOS-SCR, whereas the embedded SCR structure provides excellent ESD protection capability. What happens inside an LDMOS to develop an embedded SCR?

II. DEVICES LAYOUT

In this study, an nLDMOS was used to create different modulations on the drain side, to explore the use of a parasitic SCR for ESD reliability improvement. The experimentally tested samples were fabricated using a 0.18 μm 40 V bipolar-CMOS-DMOS (BCD) process. The channel length (L) of each nLDMOS was 3 μm, the unit channel width (W_f) was 75 μm, and the total width (W_{tot}) was 450 μm (finger number M = 6). And, all the cell area (guard-ring included) of these tested chips was kept same as 202.72 × 126 μm^2. Figs. 1 and 2 depict the cross-

section structure and schematic layout of a high-voltage (40 V) nLDMOS; this sample was defined as the experimental reference device (Ref. DUT). The drain side in the second tested device group (DUT-2) was divided into left, middle, and right subregions (the width was kept at 12.14 μm, 5.75 μm, 12.14 μm, respectively). The original N^+ regions of the left and right zones were removed and replaced with P^+ dosages. The intermediate region remained an N^+ region, forming an LDMOS-SCR (pnp arrangement), as shown in Fig 3. In the third device structure (DUT-3), the middle region (N^+) of the drain end of the DUT-2 was removed, and the left and right areas remained P^+ doped, forming a pure SCR, as shown in Fig. 4. In the fourth device structure (DUT-4), the left and right (P^+) regions of the drain end of the DUT-2 were removed. In other words, the N^+ area on the drain side was reduced, forming a pure nLDMOS (DUT-4), as shown in Fig. 5.

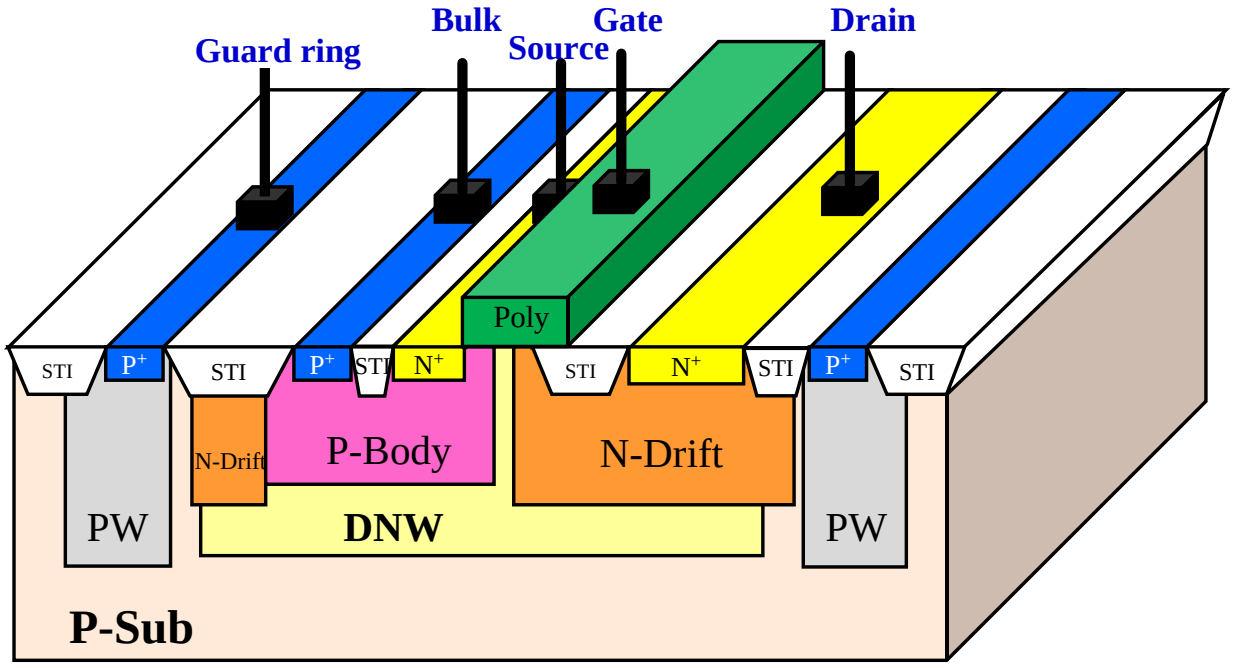

Fig.1. Cross-sectional view of an nLDMOS (Ref.; DUT-1).

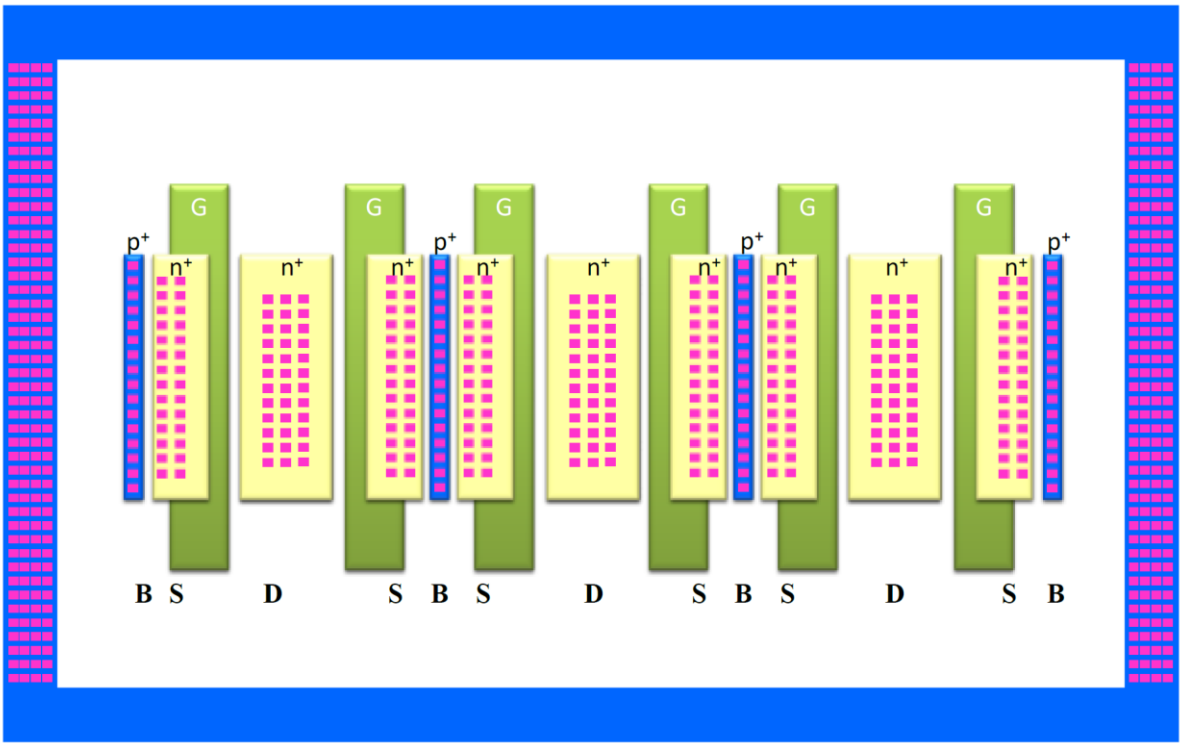

Fig.2. Schematic layout of an nLDMOS (Ref.; DUT-1).

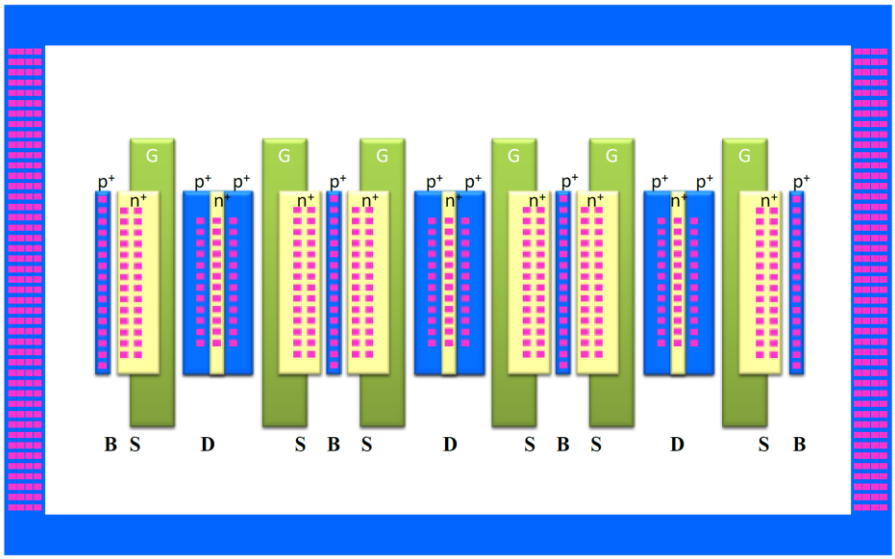

Fig.3. Schematic layout of an nLDMOS-SCR (pnp; DUT-2).

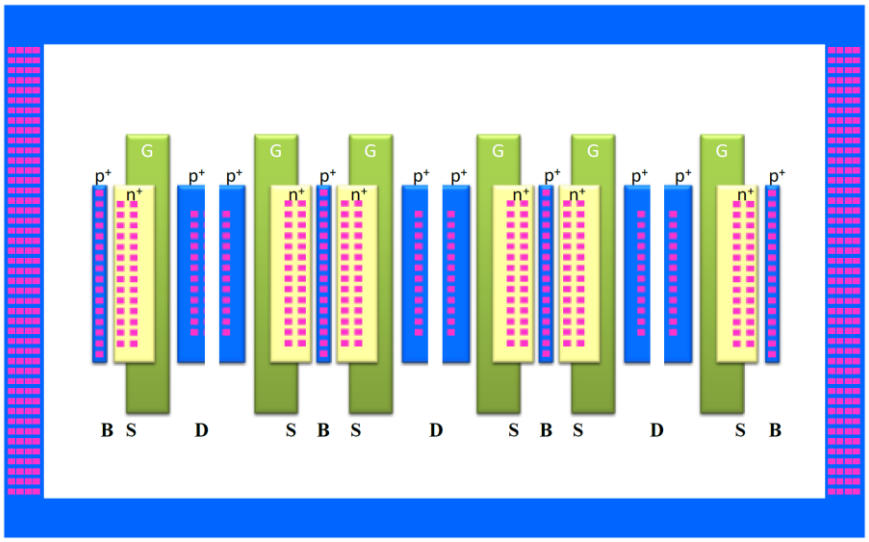

Fig.4. Schematic layout of the pure SCR (DUT-3) translated from the nLDMOS-SCR (pnp).

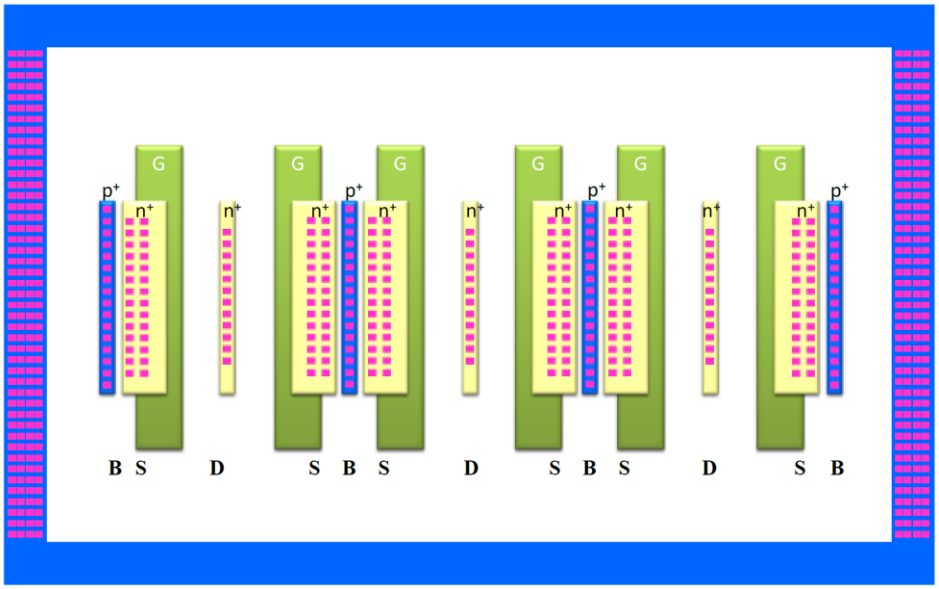

Fig.5. Schematic layout of the pure nLDMOS (DUT-4) translated from the nLDMOS-SCR (pnp).

III. TRANSMISSION-PULSE TESTING SYSTEM

A transmission-line-pulse (TLP) system with human-body-model-like characteristics was used to evaluate the snapback key parameters of the nLDMOS samples. This TLP tester was operated using a convenient measurement from the LabVIEW interface, which controlled the electronic facilities of the subsystem, such as the ESD pulse generator, multichannel voltage supplier, and high-frequency digital oscilloscope. A TLP tester can provide a continuous step-high square pulse to a sample, and the rising/falling time of the continuous square wave can quickly follow the transient noise of an ESD incident. This TLP testing system used a short square wave with 100 ns pulse widths and < 10 ns rising/falling times to evaluate the I/V response of a device.

IV. MEASUREMENT RESULTS AND DISCUSSION

The samples (Ref. DUT, DUT-2~DUT-4) were tested using a TLP machine, and their snapback I-V curves and leakage–current values are shown and listed in Fig. 6 and Table 1, respectively. The testing results showed that the V_{t1} of the nLDMOS reference group was 50.374 V, and the parasitic BJT had a significant snapback phenomenon after it was triggered on (V_h = 10.598 V and I_{t2} = 2.498 A). In DUT-2, when an embedded SCR (pnp arrangement) was added into the drain side, the V_{t1} and V_h values were reduced to 43.846 V and 4.144 V, and the snapback behavior was more obvious. Moreover, the I_{t2} level increased to more than 7 A, which means that the ESD immunity increased significantly. Thus, adding P^+ zones to Ref. DUT to form SCRs (pnp arrangement) on the drain side can attain strong ESD robustness. In other words, DUT-2 has the advantages of both LDMOSs and SCRs. Figs. 7 and 8 show that, after decomposition of DUT-2 (with the nLDMOS and SCR devices composited in parallel), compared with the pure SCR (DUT-3) and nLDMOS-SCR (pnp), the pure SCR (DUT-3) had a much lower V_{t1}, but its I_{t2} was still high (>7 A). Furthermore, the V_{t1} of the pure nLDMOS (DUT-4) was more than 100 V, and the V_h was also obviously increased; particularly, the I_{t2} value (3.043 A) of DUT-4 was higher than that of Ref. DUT.

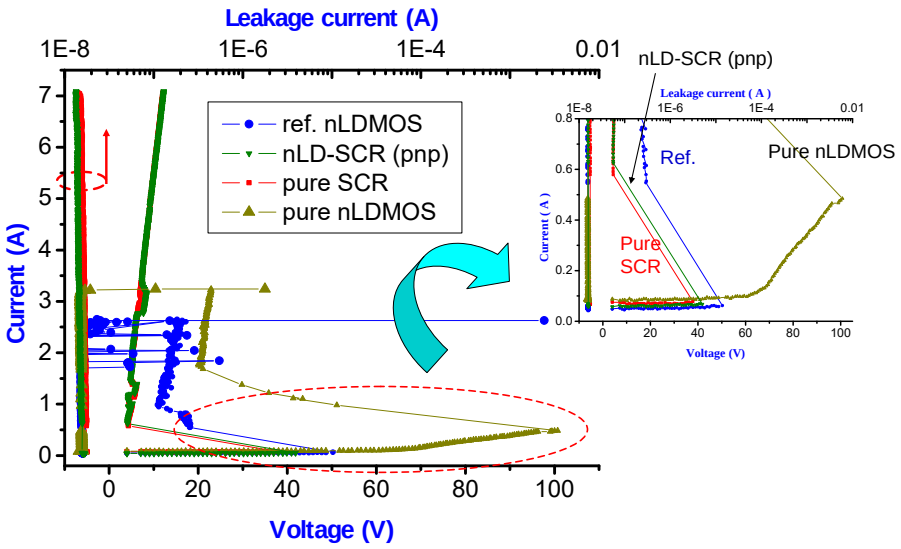

Fig.6. Snapback I-V curves & leakage currents of the tested samples.

		V_{t1} (V)	V_h (V)	$I_{t2} \pm \sigma$ (A)
Ref. DUT (nLDMOS)		50.374	10.598	2.498 ± 0.274
nLDMOS-SCR (*pnp*)		43.846	4.144	> 7
nLD-SCR (*pnp*)	**Pure SCR**	38.215	4.381	> 7
	Pure nLDMOS	100.884	20.186	3.043 ± 0.309

Table 1: Snapback key parameters of the tested samples (σ was calculated by 3 DUTs)

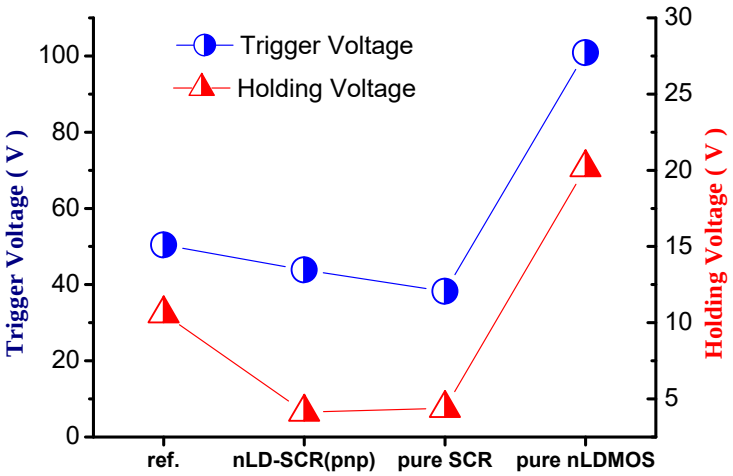

Fig.7. Relationship diagrams of V_{t1} & V_h of the tested samples.

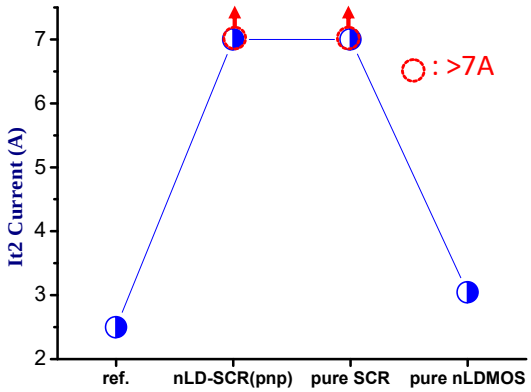

Fig.8. Relationship diagram of It2 values of the tested samples.

Generally, the nLDMOS-SCR is a complex and composited device, which can be regarded as a pure SCR (DUT-3) connected in parallel with the pure nLDMOS (DUT4) shown in Fig. 9. To further explain the good ESD-reliability capability of the nLDMOS-SCR (pnp arrangement), we first analyzed the parasitic SCR (DUT-3) and pure nLDMOS (DUT-4) of this composite device. The parasitic equivalent circuit of the pure SCR (DUT-3) device; here, the pure SCR was composed of two parasitic BJTs beneath the device. The bases of these two BJTs were connected to each other's collector; thus, the conduction of one BJT affects that of the other, which results in a positive feedback effect. Eventually, the on-resistance (R_{on}) value was very low after conducting the entire system, it could produce high driving current capability, and the holding voltage was very low. The trigger voltage V_{t1} is related to $R_{N\text{-}Drift\&DNW}$ and $R_{P\text{-}Body}$, and the V_{t1} value is lower than that of Ref. DUT, which can also be verified by the low V_{t1} value of the pure SCR (DUT-3) in Table 1.

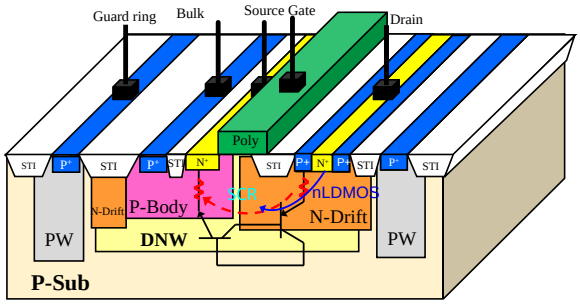

Fig.9. Parasitic equivalent circuit of the nLDMOS-SCR (pnp) device.

V. CONCLUSIONS

In this study, the ESD protection level of the reference nLDMOS was not satisfactory (I_{t2} value of only 2.498 A). The I_{t2} value could be increased to 7 A by using an embedded SCR (pnp arrangement) on the drain side. Compared with Ref. DUT, this represents an I_{t2} increase of more than 180%. In addition, after decomposition of the nLDMOS-SCR (pnp; DUT-2), the V_{t1} value of the pure SCR (DUT-3) was the

lowest. The I_{t2} of the pure SCR could also reach 7 A. The R_{on} value of the pure nLDMOS (DUT-4) increased because of the increase in R_{STI}; thus, the V_{t1} value of DUT-4 was as high as 100.884 V. Nevertheless, the I_{t2} value can be increased to 3.043 A in this pure nLDMOS. Compared with Ref. DUT, the ESD protection capability of the pure nLDMOS (DUT-4) was increased by approximately 21%. Finally, the nLDMOS-SCR (pnp arrangement) had the high driving current of the pure SCR (DUT-3) and the high V_{t1} and V_h characteristics of the pure nLDMOS (DUT-4).

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