CODE-DRIVEN BOUNDARY SCAN TESTING

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Abstract- During the last few years, integrated circuits (ICs) manufacturing was developed to be more compatible with "Design for Testability (DFT)" features. New embedded circuits were interpolated inside IC wafers. Such new additions increased the IC design complexity and as a result, the manufacturing overheads also increased. In this paper we introduce a new technique for testing onboard ICs with less embedded circuitry inside chips. The new technique depends basically on driving the test process by test code packets. The transmitted test packets have meaningful compartmentalized pieces of information which are capable to control all test activities. Test access port (TAP) is to be excluded from IC circuitry and shared over the board to serve all ICs together. TAP units activities are totally subjected to the data packet instructions. The design is simulated by NI Multisim software.

Keywords- Integrated Circuits (ICs), Design for Testability (DFT), Test Code Packets, Test Access Port (TAP)

I. INTRODUCTION

During IC manufacturing, testing forms an important step in quality insurance before marketing. Also for the last consumer, IC testability feature is a pivotal issue when selecting proper device. This feature offers more reassurance for future device maintenance capability.

Traditional testing techniques became incompetent in keeping up with the rapid IC manufacturing development. The IC incredible shrinking and the design enormous complexity increments are the two main factors which caused the deficiency in traditional testing methods. The dependence on direct contact between tester nails and IC pins became impossible.

In 1985, Joint Test Action Group (JTAG) was founded. Its main objective is to standardize IC boundary scan testing. In 1990, the group combined with IEEE community to be formally known as IEEE 1149.1 Std. The standard outlines the DFT integrated circuit design. It mainly focuses on embedding additional circuitry in IC to interface test systems via in/out pins. The main units to be added for ICs are bypass register, identification register, boundary scan register, instruction register and TAP controller as shown in Figure 1.

The main goal of using TAP is to control the data flow between the debug and test system (DTS) and the target system (TS) logic core. The data distribution is based on the instruction register (IR). TAP receives binary codes via test mode select (TMS) pin and routes the data according to instruction register commands. Also, the corresponding test data output (TDO) has to pass through TAP before exiting to DTS. IEEE 1149.1 compliant TAP is called TAP.1. Primarily it has four essential in/out pins and one optional; test data input (TDI), test mode select (TMS), test clock (TCK), TDO, and the optional pin test rest (TRST). The testing procedure follows the serial input binary data of TMS pin. Initially, TMS signal activates IR. The captured value of IR determines which register to be selected later [6, 7].

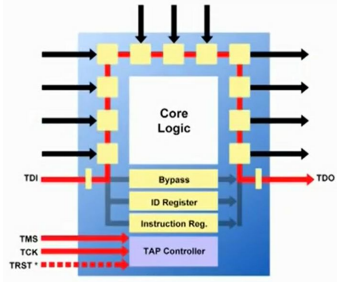


Figure 1: 1149.1 Compliant IC

The TAP controller initializes the Test-Logic-Reset state. While TMS remains a 1, the state remains unchanged. In the Test-Logic-Reset state and the active register is determined by the contents of the Instruction register. The selected register is either the Identification register, if present, else the Bypass registers. Pulling TMS low causes a transition to the Run-Test/Idle state. Figure 2 represents the timing diagram of TAP.1 [8].

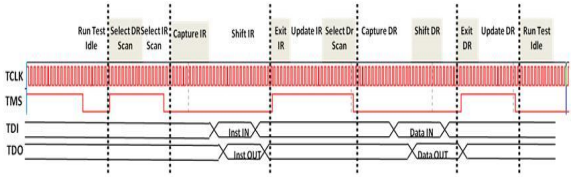


Figure 2: IEEE 1149.1 test timing sequence diagram

In 2009, a new IEEE extended standard was disclosed. It's called IEEE 1149.7 Std. The main motivation for developing such standard is to reduce pins count. To

achieve this, the embedded circuitry was upgraded and new units were also added. As seen in Figure 3, an intellectual property is to be integrated with IEEE 1149.1 Std circuitry to form what's called TAP.7. These units are located between IEEE 1149.1 logic units and target system logic [9-11].

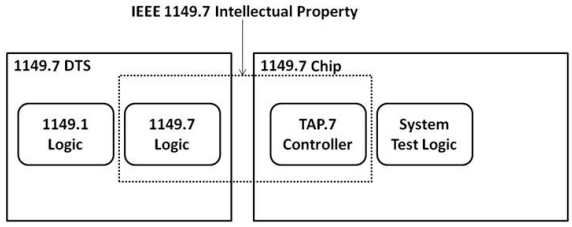


Figure 3: IEEE 1149.7 intellectual property

Unluckily, reducing pins count in TAP.7 was not free of charge. Three extra units have to be appended compulsively to each TAP circuitry. Those extra units are: Advanced Protocol Unit (APU), Extended Protocol Unit (EPU) and Reset and Selection Unit (RSU) (see Figure 4).

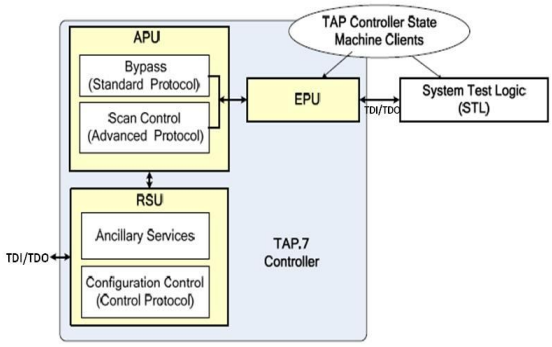


Figure 4: TAP.7 main units

Based on the aforementioned, IC design became more and more complex since of boundary scan test circuitry additions. Although IEEE standard facilitates testing procedure, IC manufacturing overheads increased proportionally. Moreover, the multiple wire (pin) interfaces poses another dilemma since it increases printed circuit board (PCB) traces interference.

Thus, there is a need in the art for a testing method that doesn't require adding exaggerated circuits to each chip, so we can diminish the resulting irrational overheads and IC design complexity. Furthermore, there is a need for a technique that uses the star topology connection to avoid any functional deficiency of the daisy-chained connection. There is a further requirement that the TAP is being shared for all onboard-chips to decrease anymore power consumption caused by embedding TAP inside each chip.

The proposed method based on sharing TAP over PCB. The data transmitted to that board will be in form of information packets. TAP redirects data to its destination according to the packet contents. Hence, the data packet doesn't only contain TDI, it also includes control bits which drive and guide TAP. Only one TAP is to be placed onboard controlling all the test process. Only boundary scan registers are to be embedded in the chips; other circuits are excluded from the proposed design.

II. TEST DATA PACKET

The proposed test data packet is a formatted unit of data that will be carried by a shared TAP. The data packet format is designed to be comprehensive enough to involve data information such as TDI and control information such as IC address, TDI length and TDO length. With the proposed data packets there is no need to customize TAP for each chip, it is enough to share one TAP for all chips on board. Information that is included in the proposed scan packet (SP) drives totally all TAP units' activities. The scan packet is represented in Figure 5.



Figure 5: The proposed scan packet format

As seen in Figure 5, SP control information contains two types of data, the "directive" and "stall" data. Directive data is the sequence of bits that causes an action which effects TAP controller. Stall data is a sequence of bits that causes a delay in the test process waiting the completion of present task. IC address is an example of directive data while TDI length and TDO length is an example of stall data.

Because of TAP sharing, the address of DUT has to be declared in each SP. This guides TAP to open the intended communication port with the target DUT. Immediately, after opening communication port, TDI starts flowing toward DUT.

The transmission period of TDI is restricted by the value TDI length. Hence, a counter circuit is designed to control the period of TDI transmission.

Accordingly, TDO will be received by TAP. A reception counter also designed to control TDO reception period according to the value of TDO length. The process repeats sequentially to allow transmission of all TDI patterns and recognizing all corresponding TDO. Henceforth, unlike IEEE 1149.1 Std, DTS is the source of all generated control information and the shared TAP has been exempted from this task. The timing diagram of scan packet is illustrated in Figure 6.

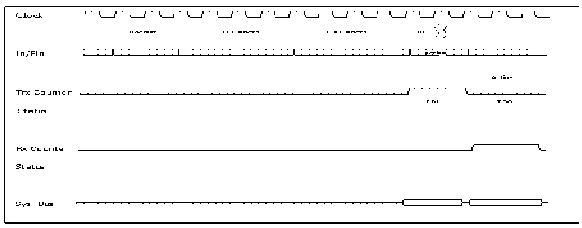


Figure 6: Timing diagram of scan packet

III. IC ADDRESS

The IC address word determines which IC to be tested. It comprises of a number of bits according to maximum number of DUT on the board. The address word will be processed by a switching circuit to open the associated port. The circuit basically depends on de-multiplexing the address word. Hence, if we have (N) ICs to be tested, then the number of address bits is (Log2N).

Switching circuit is a method which sets up a limited number of ICs connections of constant bit rate and constant delay between TAP and ICs for exclusive use during the testing session. Each IC connected to a switch port can send/receive data to/from TAP at a time, and the transmissions will not interfere with the limitation that, in half duplex mode, each line can only either receive from or transmit to TAP at a certain time. Figure 7 bellow describes forwarding of TDI and TDO according to the address word.

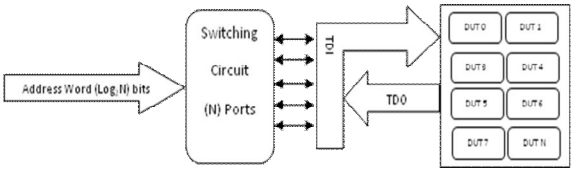


Figure 7: Processing address word by a switching circuit

IV. TDI LENGTH

TDI length code determines the period of TDI Transmission from TAP to the target system. It will be introduced to a binary counter as its initial value. The counter starts counting down starting from this value till (0) value. During counting period, the counter is generating a signal that allows TDI permeation toward IC. At the moment at which counting reaches zero value, the transmission port is closed and the reception port is opened to receive the response pattern from the TS.

V. TDO LENGTH

TDO length code determines the waiting period for TDO exiting. This code is introduced to another binary counter as its initial value. The reception port will be closed at the moment the binary counting reaches to zero value. Then immediately, the transmission port has to be opened or the circuit resets to interface a new DUT. The action of TDI and TDO length code in TAP circuit is drawn in Figure 8.

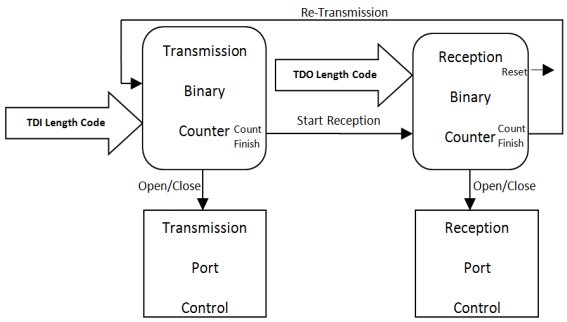


Figure 8: TDI and TDO length code action block diagram

VI. TDI CODE

It is the test pattern that is intended to be applied on DUT inputs. The length of TDI varies according the DUT. At all cases, the TDI length must be compatible with the predetermined length. TDI pattern passes through one trace toward DUT and the header must be (1) as a start indicator. Test pattern is received by a boundary scan circuit in DUT, it will be applied synchronously on all device inputs. Our design allows transmitting several test patterns sequentially without the need of resending DUT address each time. The timing diagram of TDI/TDO exchange is represented in Figure 9.

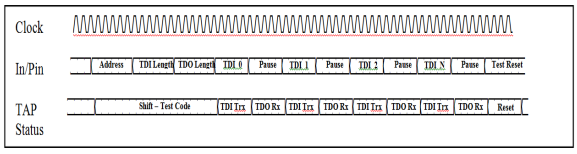


Figure 9: Transmitting TDI and Receiving TDO timing diagram

One of The most important features in our design is that TDI and TDO employ the same data line. Such feature decreases the number of lines between TAP and DUTs to its minimal value. Therefore, the circuit complexity and design overheads are significantly decreased.

CONCLUSION

The new design which is based on code-driven testing minimizes the circuit complexity and design overheads since it utilizes only one shared TAP instead of multiple TAPs. The system units change its state according to the received test code. No memory is required on the design; the DUT is pre-identified by the test code. One data trace is required to transmit and receive TDI and TDO between TAP and DUT. The direction of data is controlled by special units which are also driven by the test code. The test data is formatted as information packets to include control and data information.

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