DESIGN OF A CURRENT STARVED RING OSCILLATOR FOR PHASE LOCKED LOOP (PLL)

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Abstract- This paper presents a five and three stages current starved Voltage Controlled Oscillator (CMOS VCO) for low power Phase Lock Loop (PLL). The implemented design used a standard 0.18µm CMOS Technology with simulation CAD software mentor graphics tool. uses two models of P-channel and N-channel Mosfets Model I and II. The Model I and II of P-channel. The experimental results presentented suggests that the designed exibits twoVCO frequency ranging from 21MHz to 315.34 MHz at low power. The designed circuit is simulated using 180nm SCN018 Technology, and the product of this current and voltage approximate the power consumption to be 105.3mW, the procedures of the system design are illustrated step by step in this paper. The proposed design is suitable for PLL as a frequency multiplier based on its features as presented.

Keywords- Low Power, Current Starved VCO, PLL, CMOS Technology, Mentor Graphics Tool, Phase-Locked Loop

I. INTRODUCTION

Phase locked loops (PLLs) are common applications for VCOs based frequency synthesiser isusually used in RF transceivers.[3] There are three types of PLL, namely, an analog PLL, digital PLL, and all-digital PLL.A given PLL can be implemented in various different architectures. PLLs can be used for clock generations, such as in a microprocessor, clock and data recovery, such as in an optical transmission system, or frequency synthesis, such as in a wireless radio. The general characteristic for VCOs used in PLLs is wide tuning range so that the entire frequency range is covered. Also the phase noise requirement of the VCO can be loosened due to that when the loop is locked, the noise generated by the VCO at the center of oscillation frequency will be filtered out by the loop bandwidth. As a result, PLLs generally use wide tuning range and noisier ring topology VCO.

II. PLL ARCHITECTURE

A basic block diagram of PLL is introduced in Fig 1. It consist five main blocks [7]
1) Phase/Frequency Detector (PFD)
2) Charge Pump (CP)
3) Low Pass Filter
4) Voltage Controlled Oscillator (VCO)
5) Counter to Divided by N.

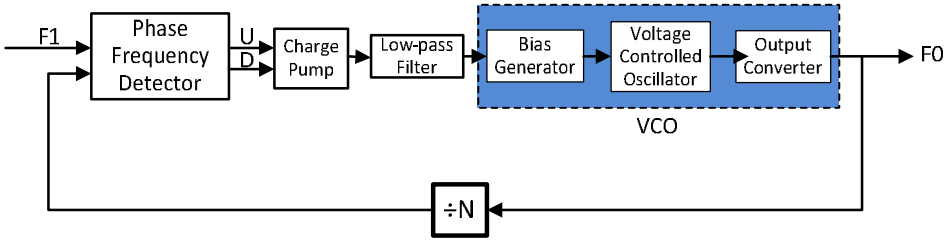


Figure 1: PLL Architecture

Figure 1 Illustrated the Phase-Locked Loop consist of Phase/Frequency Detector(PFD), charge pump (CP), low pass filter (LPF), Voltage ControlledOscillator (VCO) and frequency divider. This paper attemps to improve the current starved VCO to cover a wider range frequency at low power comsumption.

A. Background of VCO

The key metrics of a VCO consist of: oscillation frequency, tuning range, phasenoise, and power consumption.the voltage controlled oscillator (VCO) is a key component in successful broadband receivers, mainly in the receiver front end where noise can have a dramatic effect upon the quality of a broadband signal coming from an antenna or digital TV cable. Careful VCO design is needed to cope with tuning over a wide range of frequencies for broadband requirements.Radio frequency (RF) circuits have traditionally been implemented using integrated bipolar technology with external passive components. More recently however, RF circuits implemented using CMOS technology have been shown to provide significant cost savings compared

to bipolar technologies.

A voltage controlled oscillator is a stratagem in which the oscillation frequency is controlled by voltage input. Voltage controlled oscillator (VCO) forms a key element in the design of high frequency component using phased locked loops (PLL).

B. Design Steps

1. The inverter sizes MOSFET of Figure 2, are calculated.
2. The capacitance is calculated as follows: [4]-[5]

C_{total} = (5/2)Cox(WPLP+WNLN)

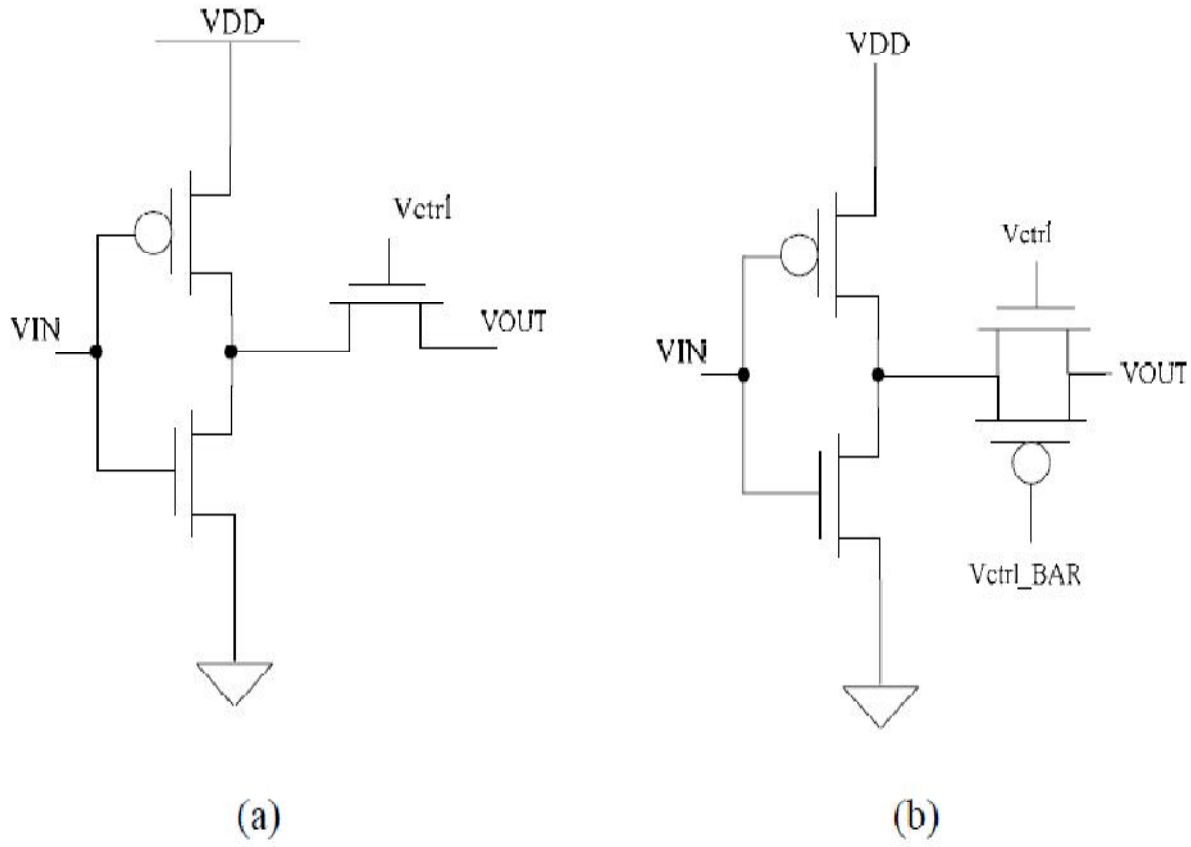


Figure 2: Inverter Schematic

C. A Ring Oscillator

Ring Oscillator consists of multiple gain stages within the loop.each gain stage can be as simple as an inverter,or as complicated as diffrential amplifire. Figure 3 show a three ring oscillator archittecture.

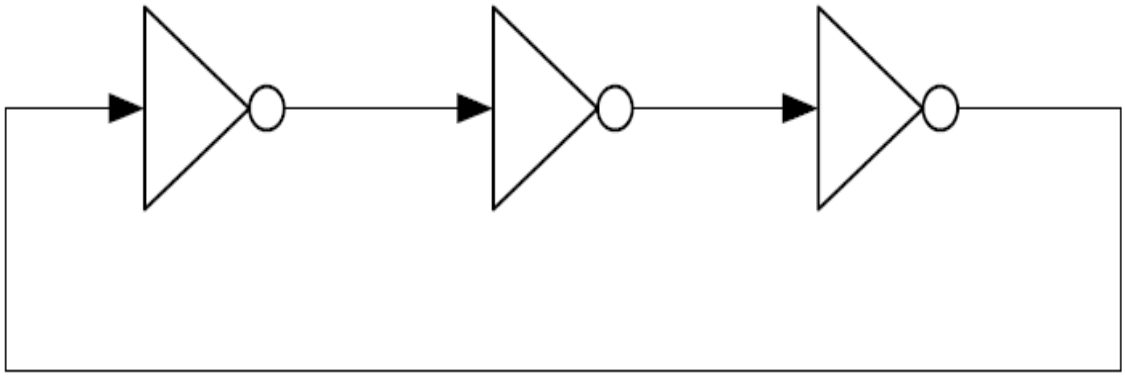


Figure 3:Three ring oscillator archittecture.

III. CURRENT-STARVED VOLTAGE CONTROLLEDOSCILLATOR

The pre-simulation waveform of current source designed presented in this paper, the powersupply voltage changes from 0.4 to 1.8V.

A. The Current Sterved VCO Circuit

In the circuit stage used as VCO, I have decided to design a Current Starved Ring Oscillator for Phase Locked Loop (PLL)which has 11 pMOS and 11 nMOS.

I'm also have success run DRC after do the layout

and at the LVS and indicated the circuit diagram and the MOS layout of the complex comparator with the result test of DRC and LVS and the simulation test results.

We have tested the W/Lvalue with 10 µm/0.5µm.

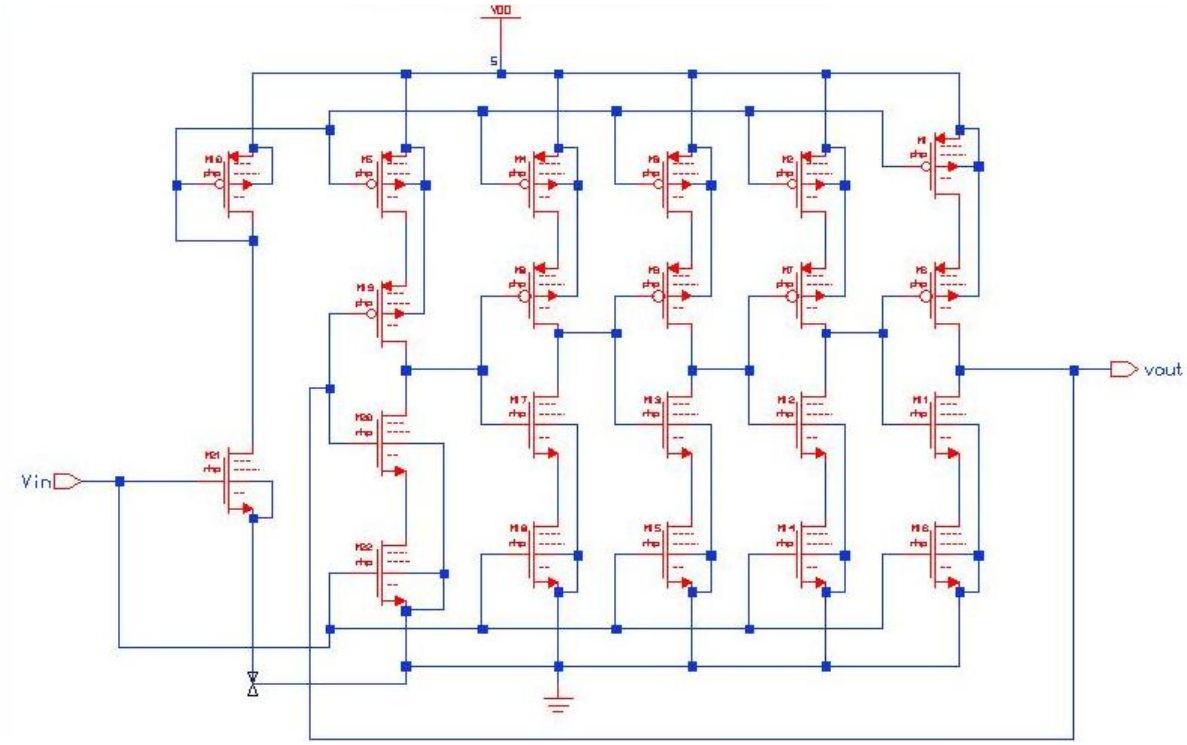


Figure 4: 5-Stage Current Sterved VCO Circuit

B. First aspect ratio setup in Designed 5-stage Ring VCO

This table show the lengh(L) and width(W).I prepare the circuit diagram acording this table.

Table 1: The first setup of the transistors W/L aspect ratios.

Devicenumber	Device type	Aspect Ratios (W/L)
M1,M2,M3,M4,M5	PMOS	10/0.5
M6,M7,M8,M9,M10,M11	PMOS	8/0.5
M12.M13,M14,M15,M16	NMOS	10/0.5
M17,M18,M19,M20,M21,M22	NMOS	8/0.5

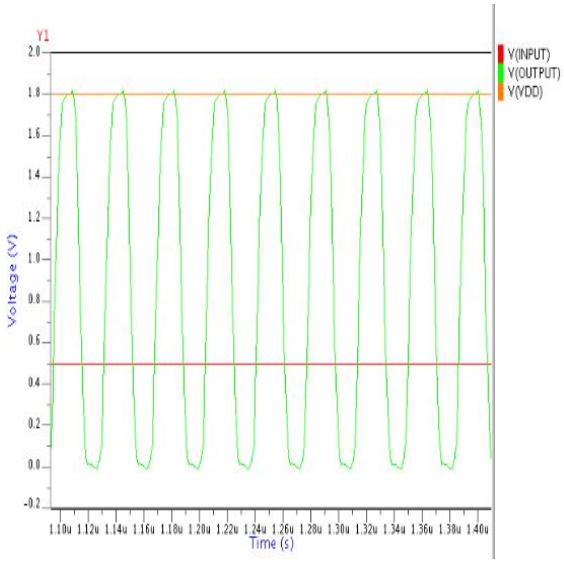


Figure. 5: VCO output frequency at 1.8V input signal

Looking at the results from Figure. 5, the highest frequency obtained at 1.8V control voltage is 33.83MHz. Table 1 shows the setup of the aspect ratio of this experiment, and the results in Table 2 shows the starting frequency from 0.4V to 1.8V control voltage.

This implies that the initial setup of the MOS devices aspect ratio needs to be adjusted for VCO higher frequency.

Table 2: The results with Control Voltage from 0.4 to 1.8V

Control Voltage (V)	Frequency(MHz)
0.4	21.32
0.5	23.05
0.6	23.29
0.7	23.57
0.8	25.67
0.9	26.30
1	26.99
1.1	27.62
1.2	28.24
1.3	28.77
1.4	29.34
1.5	29.80
1.6	31.11
1.7	32.52
1.8	33.83

C. Second Designed 3-stage Ring VCO

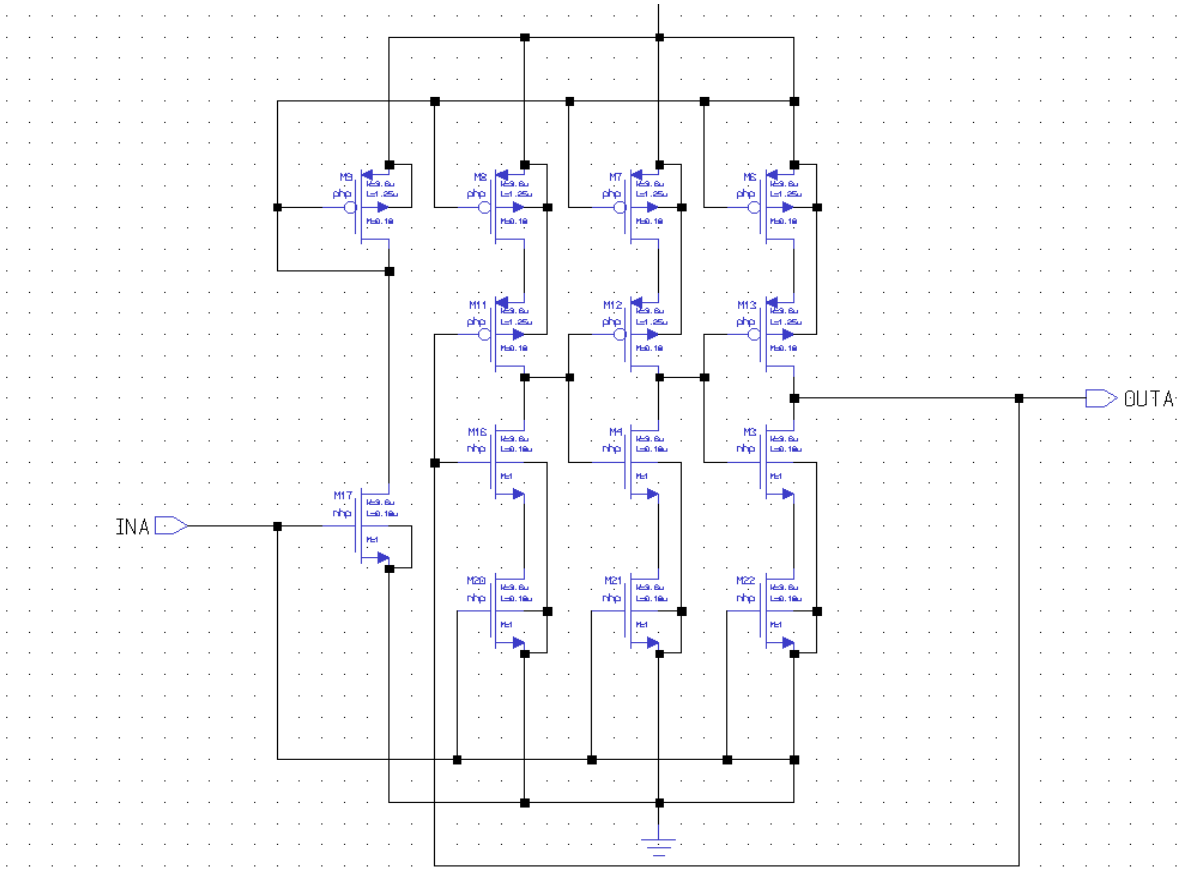


Fig.6: The designed 3-Stage Current Sterved VCO Circuit

D. Aspect ratio setup in the Modified 3-stage Ring VCO

This table show the lengh(L) and width(W).I preparedthe circuit diagram according to this table.

Table 3: The third setup of the transistors W/L aspect ratios.

Devicenumber	Device type	Aspect Ratios (W/L)
M1,M2,M3	PMOS	2.5/1.25
M4,M5M6,M7	PMOS	2.5/1.25
M8,M9,M10,M11	NMOS	2.5/1.25
M12.M13,M14	NMOS	2.5/1.25

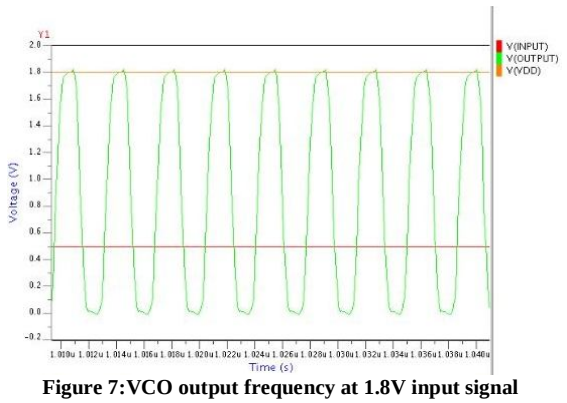


Figure 7:VCO output frequency at 1.8V input signal

Looking at the results from Figure 7, the highest frequency obtained at 1.8V control voltage is 315.54MHz. Table 3 shows the setup of the aspect ratio of this experiment, and the results in Table 4 shows the starting frequency from 0.4V to 1.8V control voltage. This implies that the initial setup of the MOS devices aspect ratio needs to be adjusted for VCO higher frequency.

Table 4: The first setup of the transistors W/L aspect ratios.

Control voltage (V)	Frequency(MHz)
0.4	159.39
0.5	167.05
0.6	171.29
0.7	178.57
0.8	188.67
1	223.99
1.1	238.62
1.4	275.34
1.5	282.14
1.6	295.39
1.7	305.17
1.8	315.54

The load transistor width were selected to be 16µm by comparing the curves in figure 9 for the maximum frequency and the stable operation ranges.the final transistor size of the single-looposcillator is given in table3.

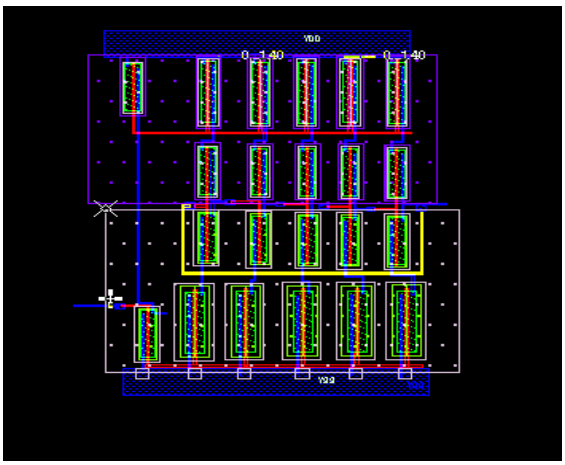


Fig8: VCO Layout

CONCLUSION

A simple 5-stage and 3-stage ring VCO been designed.The complete circuitry of the designed VCO has been implemented using the 0.18umCMOS technology.The simulated results of the voltage source VCO proposed is suppliled in 0.1V step change starting from 0.4 to 1.8V. After extract the parasitic parameters of layoutand simulations, a detailed comparison between the existing work and the proposed low power ring VCO, the results showed that the frequency and the power obtained with our 3-stage deisgned ring VCO exibits better performance in comparison to the existing. The VCO has been designed with low power, small chip size area and better using 180 nm CMOS technology for high performance. While increasing the number of stages for getting the higher frequency the power dissipation and size of oscillator was going to increase.

Hence instead of increasing the number of stages and time constant again a control voltage and width of the CMOS can be adjusted for getting the higher frequency. This paper adopts the standard CMOS technology, therefore, the design of volatge source unit can beused for PLL and other applications the require a low power comsumption VCO at frequency rangoinh from 22 to 315MHz.

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