DESIGN OF SRAM MEMORY IN JPEG 2000 IMAGE COMPRESSION WITH MULTI BIT FLIP FLOPS

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Abstract- In this paper we propose a technique for reducing the size of memory for JPEG 2000. Generally, for storing the data Static Random Access Memory is used in JPEG 2000, after the quantization of bits. To reduce the size of memory we are considering multi bit flip flop concept with merging of flip flops concept.We also analyze the characteristics of discrete wavelet transform. The proposed system has the less complexity and the power consumption decreased significantly. Results shown that this method is very efficient in reducing the area also. Implemented the system with Xilinx vertex-5 family.

Keywords- SRAM, JPEG2000, ENCODING, RDF, SBFF, MBFF

I. INTRODUCTION

JPEG2000 is an emerging standard for still image compression. As digital imagery more complex and high quality, there is to manipulate more and more data. Thus image compression must not only reduce the necessary storage and bandwidth requirements, but also allow attraction for editing, processing and targeting particular devices and applications. The JPEG 2000 image compression system has a rate-distortion advantage over the original JPEG. More importantly, it also allows extraction of different resolutions, pixel fidelities, and regions of interest, components and more, all from a single compressed bit stream.

Generally for the storage of bits in encoding process of JPEG2000 Static random access memory (SRAM) will be used. An SRAM is designed to fill two needs: to provide a direct interface with the CPU at speeds not attainable by dynamic random access memory (DRAM) s and to replace DRAMs in systems that require very low power consumption. In the first role, the SRAM serves as cache memory, interfacing between DRAMs and the CPU.

While storing the data in this static random access memory it can suffer errors due to some doping of metal oxide semi conductor transistors. This are called as random dopant fluctuations. Not only due to random dopant fluctuations but also due to the variations in the Threshold voltage. And also the power and propagation delay depends up on the clock distribution because the clock will have the high switching activity. Here in this paper we propose a system for random access memory for the temporary storage which will have the multi bit flip flop in place of single bit flip flop.

The proposed system reduces the area, power and transition time sufficiently. For high performance JPEG2000 architecture, a QCB based DWT method is proposed to achieve high Parallelism in the JPEG2000 coprocessor for reducing the memory size. In JPEG2000, If we process static images like pictures, Huffman encoding is enough, but if we operate the JPEG2000 for video transmission, Huffman encoder is not sufficient because videos are transmitted at frames. So if the clock frequency is high, then the dynamic images can be processed. For this case, JPEG based on entropy coder will be sufficient. For JPEG2000 architecture, it uses an efficient 2-D DWT that is capable of computing four coefficients per clock cycle. Memory is the main issue to store the number of images and videos.

Memory used basically SRAM because the primary advantage of an SRAM over DRAM is its speed. The fastest DRAMs on the market still require five to ten processor clock cycles to access the first bit of data. Although features such as EDO and fast page mode have improved the speed with which sub-sequent bits of data can be accessed, bus performance and other limitations mean the processor must wait for data coming from DRAM. Fast, synchronous SRAMs can operate at processor speeds of 250 MHz and beyond, with access and cycle times equal to the clock cycle used by the processor. With a well designed cache using ultra-fast SRAMs, conditions in which the processor has to wait for a DRAM access become rare. SRAM is also having further advantages like Density, Volatility, cost, custom features. Because of the way DRAM and SRAM memory cells designed, readily available DRAMs have significantly higher densities than the largest SRAMs. While SRAM memory cells require more space on the silicon chip, they have other advantages that translate directly into improved performance. Unlike DRAMs, SRAM cells do not need to be refreshed. This paper schedules as the section 2 describes about the JPEG 2000. Section 3 describes about the discrete wavelet transform. Section 4 discuss about the multi bit flip flop. Section 5 shows the simulation results. Section 6 concludes the paper.

II. JPEG 2000

JPEG and JPEG 2000 are the most widely used image compression standards in compensating memory errors. JPEG has slightly less compression performance than JPEG2000. JPEG is based on discrete cosine transform, where as JPEG is based on discrete wavelet transform. Where each sub band is divided into rectangular blocks, called code-blocks. DWT provides less computational complexity which can compensate memory errors drastically.

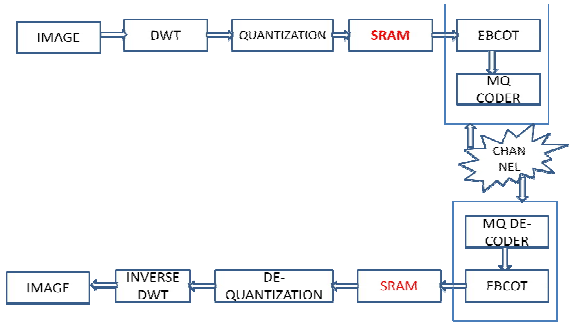


Fig. 1

The figure 1 shows the block diagram of the JPEG2000.The original image (in pixel domain) is transformed into frequency sub-bands using the DWT engine followed by quantization and stored into the SRAM memory. Compressed image is obtained after embedded block coding with optimal truncation processing, followed by rate control.

III. DISCRETE WAVELET TRANSFORM

The two level sub-band representation of the DWT output is shown in figure 2. The input image of size N*N is processed by high pass and low pass filters as shown in the figure 3. Along rows and columns followed by sub sampling to generate the first level outputs HL1, HH1, LH1, and LL1. Each of size (N/2)*(N/2). The LL1 further processed by high pass and low pass filters along the rows and columns to generate the second level outputs HH2, HL2, LH2 and LL2. Each of which is of size (N/4)*(N/4). For a natural image, a low frequency sub-bands are likely to contain coefficients with larger values while higher frequency sub-bands such as HL1, HH1, and LH1 contains co efficient with small values. Moreover, the coefficients ina sub-band have similar magnitudes. We exploit these facts in developing the memory error compensation techniques.

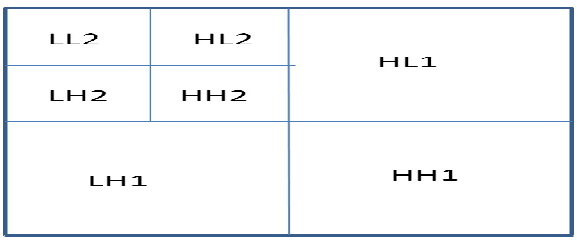


Fig. 2

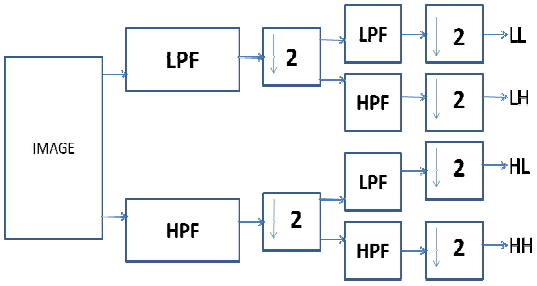


Fig. 3

IV. MULTI BIT FLIP FLOP

For the storage of Static Random access memory generally using the flip flops. Here in our paper we are proposing a multi bit flip flop in place of single bit flip flop. Optimizations in VLSI have been done on three factors: Area, Power and Timing. Speed optimization means reducing the space of logic which occupy on the die. This is done in both front-end and back end of design. In front-end design, proper description of simplified Boolean expression and removing unused states will lead to minimize the gate/transistor utilization. Partitions, Floor planning, Placement and routing are performed in back-end of the design which is done by CAD tool. The CAD tool has a specific algorithm for each process to produce an area efficient design similar to power optimization. Power optimization is to reduce the power dissipation of the design which suffers by operating voltage, operating frequency and switching activity. The first two factors are merely specified in design constraints but switching activity is a parameter which varies dynamically, based on the way which designs the logic and input vectors.

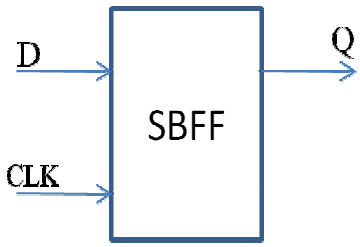


Fig. 4

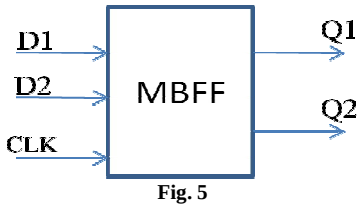


Fig. 5

The proposed method is based on the merging of clock pulse. Normally the clocks will be made by using inverter based clock buffers. In the case of multi-bit flip-flop technique the clockpower is reduced by replacing the available flip-flops withthe multi-bit flip-flops. To achieve this no of clock buffershave to reduce. To reduce the number of clock

buffer theconcept of sharing of the clock buffers by several flip-flopscan be used. Figure 6 and figure 7 shows the two 1-bit flip-flops, if it isreplaced by a 2-bit flip-flop. In this circuit the individualclock is replaced by a single clock buffer. So the two 1-bitflip-flops can share the same clock.

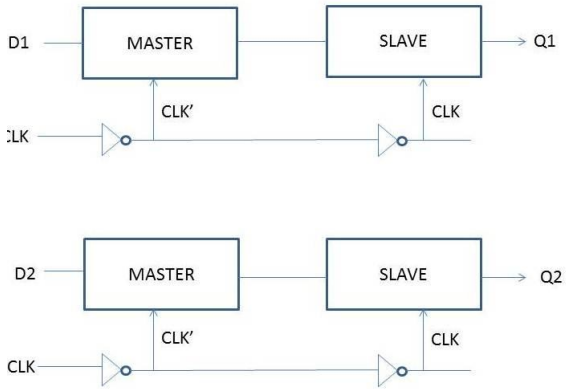


Fig.6 individual single bit flip flops

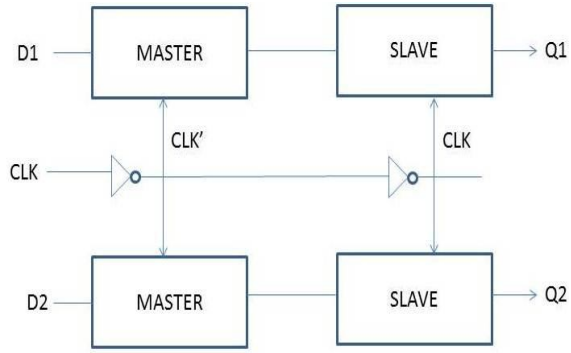


Fig. 7 Multi bit flip flop

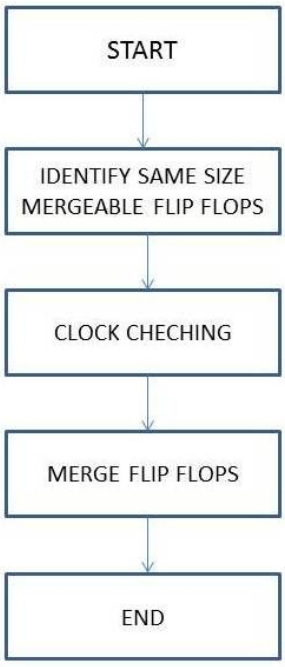


Fig. 8 Flow chart of multi bit flip flop concept

Figure 8 represents the flow chart for the multi bit flip flop concept. First we select the flip flops which are mergable and of same size. After selecting the flip flops, we will give same clock to the flip flops. This concept will be useful in storing of bits efficiently.

V. SIMULATION RESULTS

Figure 9 shows the block diagram of JPEG2000 SRAM by using multi bit flip flop. The design is implemented in Xilinx 10.1 version. Code is written in verilog hardware description language. Figure 10 represents RTL view of JPEG 2000. Figure 11 shows the power results for the jpeg2000. Power decreased by 42% when compared with the single bit flip flop.

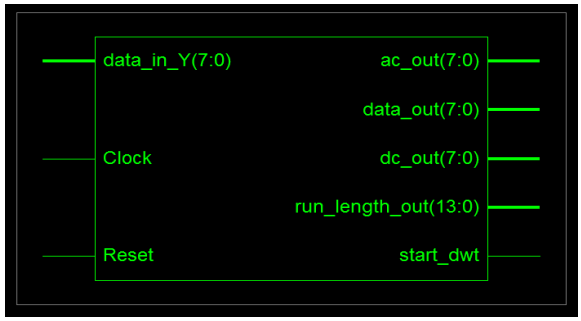


Fig. 9 block diagram of JPEG2000 SRAM by using multi bit flip flop

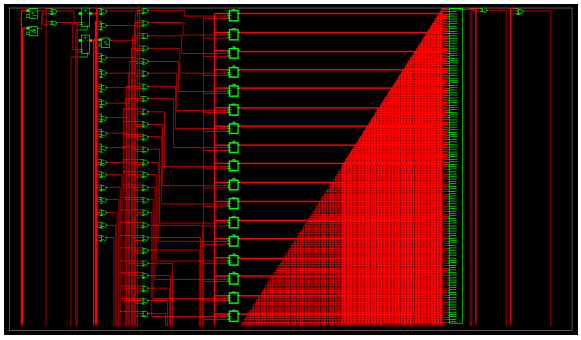


Figure 10 RTL view of JPEG 2000 SRAM

Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.000	1	--	--
Logic	0.000	536	9312	5.8
Signals	0.000	1014	--	--
IOs	0.000	49	66	74.2
Total Quiescent Power	0.080			
Total Dynamic Power	0.000			
Total Power	0.080			

Figure 11 power results of JPEG2000

CONCLUSION

We have designed a multi bit flip flop for the use of storage in JPEG2000 image compression. We analyzed the power and speed results of multi bit flip flop design over the single bit flip flop. Which can efficiently reduce the power by 42%. This design can rectify finally the errors arising in the Static Random access memory while the process of image compression is going on. And also the area using by the system decreases because the number of flip flops usage also decreases.

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