DESIGN OF A RECONFIGURABLE ARCHITECTURE FOR 2-D DWT USING PIPELINE ARCHITECTURE

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Abstract- In this novel, the proposed reconfigurable architecture is designed by using lifting method instead of convolution method. Lifting method reduces considerable hardware and computational complexity where hardware resources are major components of DWT.

Keywords- DWT; Pipeline architecture

I. INTRODUCTION

Wavelet transform is introduced by Mallat where decomposition of samples into basic functions called wavelets on the orthogonal basis[1]. The DWT computation is classified into two methods i.e. convolution and lifting methods.

The convolution method has better scalability and regularity. The advantages of lifting method are, 1. Lifting increase considerable speed when compared other standard design. 2. Lifting supports an in-place implementation of the fast wavelet transform, which is similar to the Fast Fourier Transform. Therefore, wavelet transform can be calculated without allocating auxiliary memory. 3. All operations within one lifting step can be done entirely parallel while the only sequential part is the order of the lifting operations. 4. Non linear wavelet transforms can easily build by using lifting method.5. Using lifting and integer-to-integer transforms, it is possible to combine bi-orthogonal wavelets with scalar quantization and still keep cubic quantization cells which are optimal like in the orthogonal case.

The lifting based pipelined architecture has lower hardware complexity and higher throughput for computation.

II. LIFTING METHOD

The main feature of the lifting-based discrete wavelet transform scheme is to break up the high-pass and low-pass wavelet filters into a sequence of smaller filters that in turn can be converted into a sequence of upper and lower triangular matrices [4].

The basic idea behind the lifting scheme is to use data correlation to remove the redundancy. The lifting algorithm can be computed in three main phases, namely: the split phase, the predict phase and the update phase, as illustrated in Fig.1.

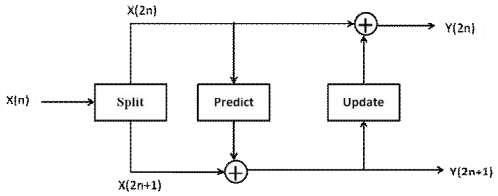


Fig.1: Split, predict and update phases of the lifting based DWT

Split phase, In this split phase, the data set x(n) is split into two subsets to separate the even samples from the odd ones:

$$Xe = X(2n),\ Xo = X(2n+1) \qquad (1)$$

Prediction phase, In the prediction stage, the main step is to eliminate redundancy left and give a more compact data representation. At this point, we will use the even subset x(2n) to predict the odd subset x(2n+1) using a prediction function P. The difference between the predicted value of the subset and the original value is processed and replaces this latter:

$$Y(2n+1) = Xo(2n+1) - P(Xe) \qquad (2)$$

Update phase. The third stage of the lifting scheme introduces the update phase. In this stage the coefficient x(2n) is lifted with the help of the neighboring wavelet coefficients. This phase is referred as the primal lifting phase or update phase:

$$Y(2n) = Y(2n+1) + U(Xe) \qquad (3)$$

Where, U is the new update operator.

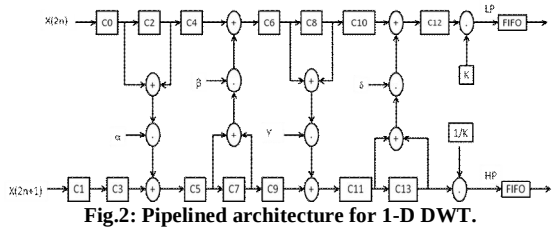


Fig.2: Pipelined architecture for 1-D DWT.

The 1-D pipelined architecture is designed by using 6 multiplier, 8 adders and 14 registers which is as

shown in fig.2. The pipeline registers depends on their relative position. The registers located before alpha multiplication in the odd dataflow and before beta multiplication in the even dataflow store integers from -127 to 128. The registers located after beta multiplication in the odd dataflow and before gamma multiplication in the even dataflow store integers from -184 to 184. The registers located after gamma multiplication in the odd dataflow and before delta multiplication in the even dataflow store integers from -205 to 205. The registers located after delta multiplication in the odd dataflow and before division by k store integers from -366 to 366. The register located at output data of the even dataflow corresponds to low frequency of input image samples store values from -298 to 298. The register located at output data of the odd dataflow corresponds to high frequency of input image samples store values from -252 to 252. These 9 bits, even though a low magnitude value is expected for this data output due to the nature of the transform of still tone images[4].

III. RECONFIGURABLE ARCHITECTURE

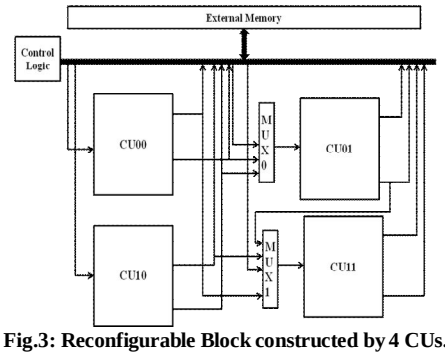


Fig.3: Reconfigurable Block constructed by 4 CUs.

A single reconfigurable block is constructed by 4 CUs, because the optimal number of CUs for processing 2-D DWT is as shown in Fig.3. The control logic controls the data flow between the external memory and the reconfigurable blocks.

The multiplexers MUX0 and MUX1 change the interconnections among CUs to reconstruct the computing circuit into different structures.

Each computing unit consist of local memory at the beginning and FIFO at the output stages respectively and MLBF(MAC Loop Based Filter).

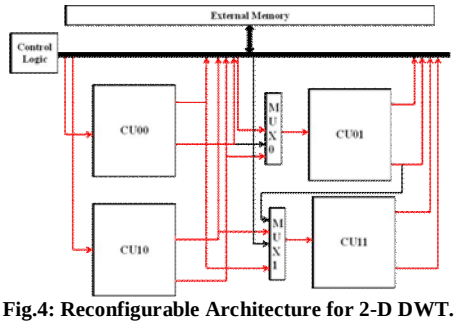


Fig.4: Reconfigurable Architecture for 2-D DWT.

The 2-D DWT on the reconfigurable Architecture has CU_{00} and CU_{10} are used as row processors, while CU_{01} and CU_{11} are used as column processors is as shown in Figure.4

IV. PROPOSED DESIGN

The same reconfigurable architecture with small change is considered i.e. Local memories at each computing units are suppressed. The input to the CUs is taken directly from the external memory.

Therefore, the memory size required is reduced compared to reference paper. Thus, it increases throughput and also by using pipeline architecture the hardware resources are also reduced.

4.1 FILTER COEFFICIENT

Coefficients	VALUE	BBRF
α	1.58613	1’.1’001’1’0
β	0.05298	0.0001’0010
γ	0.88291	0.11100000
δ	0.0.443506	0.1001’00010
κ	0.81289	0.1110001’0
1/κ	1.152344	1.0101’1’001’0

Table.1: Coefficient for Pipelined Architecture

V. SIMULATION RESULTS

]5.1 RECONFIGURABLE ARCHITECTURE

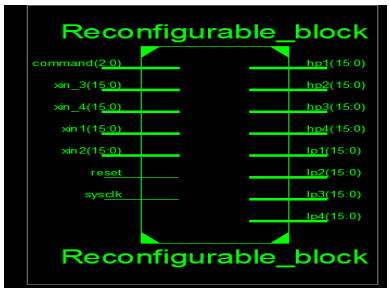


Fig.5: RTL schematic

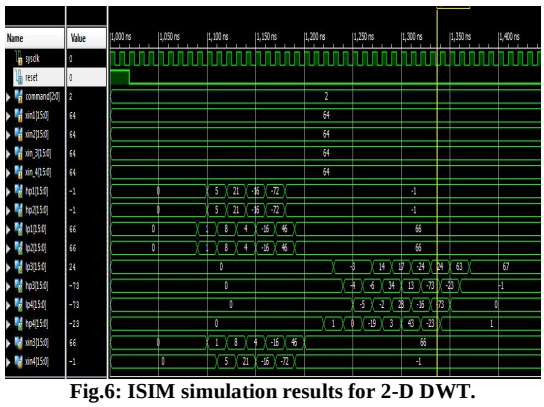


Fig.6: ISIM simulation results for 2-D DWT.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	1043	10752	9%
Number of Slice Flip Flops	1038	21504	4%
Number of 4 input LUTs	1452	21504	6%
Number of bonded IOBs	101	448	22%
Number of GCLKs	3	32	9%

Fig.7: Design Summary

Parameters	Power(W)
Dynamic	0.070
Static	0.234
Total	0.305

Table.2: Power consumed

CONCLUSION

The proposed design requires less hardware resources and also less memory than the previous work is as shown in Fig 7. Therefore, it consumes less power than the previous work is tabulated in Table2.

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