A 14-BIT 100MHZ CURRENT-STEERING DAC WITH RANDOMIZED THERMOMETER-CODING TECHNIQUE, RETURN-TO-ZERO CIRCUIT AND HYBRID LAYOUT SCHEME

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Abstract— The design of a low-cost high-speed current-steering digital-to-analog converter (DAC) is presented. On the architecture level, the randomized thermometer-coding (RTC), which offers consecutive selection, randomization, and less element switching activity, is used. Therefore, harmonic distortion caused by element mismatches can be significantly suppressed. On the circuit level, a return-to-zero (RTZ) circuit, which can isolate the DAC output nodes from the coupling of the control signals without sacrificing speed, is adopted. On the layout level, a novel hybrid layout scheme (HLS) is proposed. This scheme can compromise the quadratic and linear error distribution of systematic element-mismatch. Using the above three techniques, a 14-bit 100-MHz current-steering DAC is implemented in a 1P6M 0.18-μm 1.8-V CMOS process. The measured spurious-free dynamic range (SFDR) is higher than 80.1dB at a 100MHz sampling frequency. The measurement results show that the RTC technique improves the SFDR by more than 16dB and the RTZ circuit prevents a 15dB SFDR drop when the input signal frequency is close to half the sampling frequency. The low-cost DAC has an active area of less than 0.20-mm^2.

Index Terms— Digital-to-Analog Converter, Randomization, Return-To-Zero, Layout Scheme.

I. INTRODUCTION

Current-steering digital-to-analog converters (DACs) are widely used for wideband communications, direct digital synthesis, and video signal processing because of their high operation speed.For these applications, the most critical point for DAC design is to achieve a highspurious-free dynamic range (SFDR). In order to achieve it, the following implementation limitations must be overcame, i.e.,the static nonlinearity caused by current-cell mismatches and the dynamic nonlinearity due to output transitions.

The first limitation is themismatch of current-cell implemented by small transistors [1]. Toenable the use of small transistors, several methods have beenproposed, such as trimming, calibration and dynamic element matching (DEM) techniques [2]–[8]. Amongthem,the DEM technique requires less circuitoverhead and complexity, and thus can be effectively used for lower cost. Randomizing the selectionof current-cells to reduce mismatch effects is the main idea of the DEM techniques. Randomized thermometer-coding (RTC), which was proposed by the author in [6], firstly provides randomization and less element switching activitysimultaneously. Afterward the techniques proposed in [7] (randomswapping thermometer coding, RSTC) and [8] announce their minimum element-transition-rate. Nevertheless, the technique in [8] needs very complex implementation. In addition,RSTCdoes not fully randomizethe selection pattern because of the adjacent-element-first law,which leads to raised noise floor and humps at low frequency [8]. Therefore, the RTC technique is used in this paper. Due to the requirement of a proper layout scheme for the RTC technique, a new hybrid layout scheme (HLS) will be proposed.

The second limitation is the transient error induced by the DAC's output transition. Toreduce the nonlinearity, several return-to-zero (RTZ) methodshave been proposed. The RTZ circuit in [9] can be realizedwith large reset transistors added at the DAC output terminals, which may results in large parasitic capacitance.Without any reset transistors, the circuit in [10] can achieve higher resolution by using isolation transistors. However, the increased settling time, due to the use of isolation transistors, is in-negligible at high operation speed. In this paper, the RTZ circuit,which was proposed by the author in [11],combing reset transistorsand isolation transistors is used to overcome the second limitation.

In this paper, using the RTC, RTZ and HLS techniques, which are all proposed by the author, a low-cost high-speed high-SFDR current-steering DAC is implemented and measured.The rest of this paper is organized as follows. The RTC technique is verified and discussed for implementation in Section II. In Section III, the RTZ circuit is analyzed. Section IV presents the architecture design and circuit design of a 14-bit current-steering DAC with the proposed techniques. Measurement results are presented in Section V. Finally, conclusions are given in Section VI.

II. RANDOMIZED THERMOMETER-CODING TECHNIQUE

For a high-speed high-resolution current-steering DAC with DEM, dynamic errors should be decreased to achieve good SFDR performance. Hence, the RTC technique is used, and will be analyzed as followings.

A. Operation Principle

To maintain low switching activity, the starting element of the thermometer-coding remains unchanged for a specified number of input samples, which is defined as the randomization period (RP) [6]. For the next RP, the starting element of the thermometer-coding is randomly regenerated. Fig. 1 shows an 8-element DAC to illustrate the principle of the RTC technique with a RP of 4. DAC input codes of 7, 4, 5, 2, 6, 3, 1 and 5 were used as examples.

At the beginning, the value of SP was 0, where SP is the starting pointer of the element selection for the respective input code. As shown in Fig. 1, for RP=4 and the input of 7, elements $\{U_0, U_1, U_2, U_3, U_4, U_5, U_6\}$ were selected. For the input of 4, elements $\{U_0, U_1, U_2, U_3\}$ were selected. For the input of 5, elements $\{U_0, U_1, U_2, U_3, U_4\}$ were selected. For the input of 2, elements $\{U_0, U_1\}$ were selected.For the fifth input of 6, the SP should be regenerated randomly because one RP was completed. The SP became 6 and elements $\{U_6, U_7, U_0, U_1, U_2, U_3\}$ were selected. For the next inputs, elements were similarly selected.

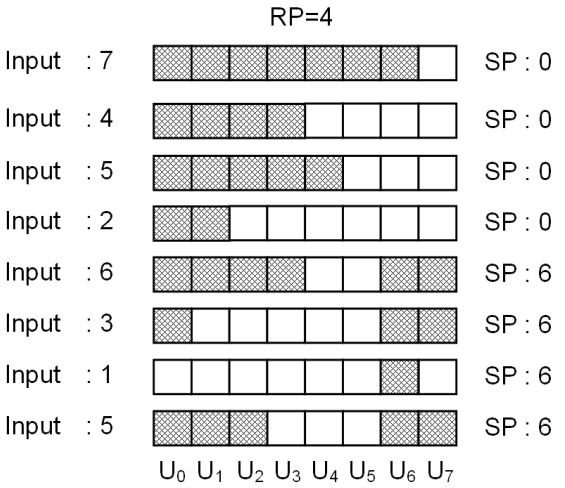


Fig. 1. Operation principles of the RTC technique for RP=4

B. Analysis, Verification and Implementation Considerations

According to [12], the DAC output can be written as y[n]=αx[n]+β+e[n], where x[n] is the DAC input, α is a constant gain, β is a DC offset, and e[n] is a conversion-error term referred to as the DAC noise. Involving the functionality of a stochastic encoder, the DAC noise tern can be re-written as $e[n] = a^T[n]e_h + \overline{a}^T[n]e_l$, where $a[n] = [a_1[n] \cdots a_N[n]]^T$ is a sequence of selection vectors generated by the stochastic encoder, $\overline{a}[n]$ represents the one's-complement of a[n] and $e_h = [e_{h_1} \cdots e_{h_N}]^T$ and $e_l = [e_{l_1} \cdots e_{l_N}]^T$ are DAC errors for $a_r[n]$=1 and $a_r[n]$=0, respectively. If a[n] is a sequence of independent random variables, e[n] will have a white spectrum and it will be uncorrelated with x[n] [12]. Therefore, the value of RP for the RTC technique will affect the shape of the white spectrum of e[n].

In order to verify the performance of the RTC technique, a 6-bit 64-element DAC is used. The element-mismatch error profile with joint error distribution (50% linear + 50% quadratic) shown in Fig. 2 is used. The error profile in Fig. 2 has an8% standard deviation. A full-scale dithered sinusoid with a frequency of (313/4096)·fs is applied to the DAC, where fs is sampling frequency. All the simulated spectra in this paper are obtained by averaging 32 periodograms, each corresponding to 213 samples. Fig. 3 shows the mismatch spectra of the DAC applying the RTC technique with RP=1, 2, 4and 8, where element mismatches shown in Fig. 2 are applied.

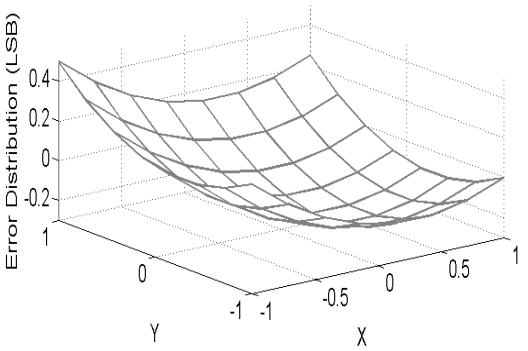


Fig. 2. A joint error distributed profile for DAC elements

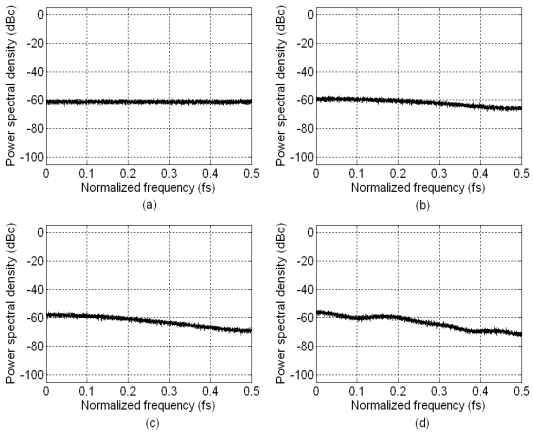


Fig. 3. Mismatch spectra of the 6-bit DAC applying the RTC technique with RP = (a)1, (b)2, (c)4, and (d)8.

The shape of the mismatch spectrum is affected by the value of RP, which introduces the randomization property to the RTC technique. Fig. 4 shows the maximum mismatch tone power and the total number of switched elements of the simulated DAC employing the RTC technique with different RPs. When the RP increases, the maximum mismatch tone power is increased while the total number of switched elements is decreased. After trading-off between the two properties of low element switching activity and randomization, RP=4 is adopted for the DAC.

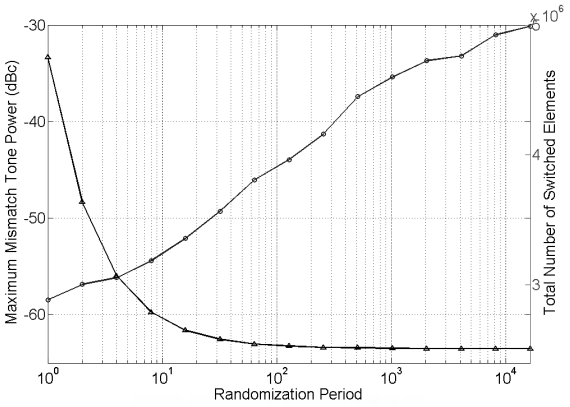


Fig. 4. The maximum mismatch tone power and the total number of switched elements of the simulated DAC employing the RTC technique with different RPs

C. Benefit of the RTC Technique's Co-use with HLS

Because the RTC technique has the consecutive selecting property, it can achieve both benefits of the DEM technique and the proper layout scheme when it is used with proper layout schemes simultaneously. Therefore, a novel layout scheme, named hybrid layout scheme (HLS), is proposed. To achieve good gradient error compensation, HLS compromises both the quadratic and linear error distribution of systematic element-mismatch.

As shown in Fig. 5(a) for sixteen elements, linear errors are compensated by following the 1 to 16 sequences. For quadratic-error compensation, when the element number is extended to 64, zones A to Dare rotated clockwise as shown in Fig. 5(b). Finally, the total switching sequence of HLS can be shown in Fig. 5(c) for the 6-bit DAC.

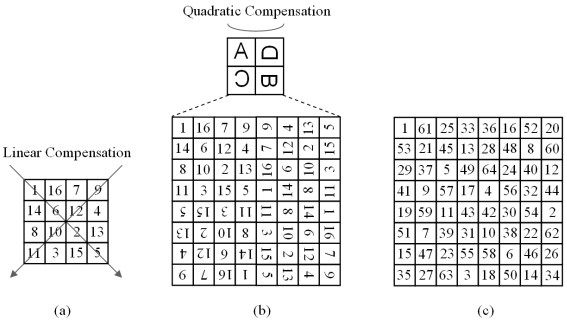


Fig. 5. Sequence arranging rule of HLS for compensating (a) linear errorand (b) quadratic error, and (c) its final switching sequence

By using HLS, the simulated INL will be about four times smaller than that of the classical switching scheme [13] based on the error profile shown in Fig. 2.Because HLS significantly suppresses the consecutively-accumulated element errors, the maximum output error for each input code of the DAC employing the RTC technique is theoretically smaller or equal to that of the DAC employing traditional randomization. Simulation results confirm the theoretically calculated results as shown in Fig. 6, where the simulation results are obtained from inputting more than 2^{20} times ramp codes to the DACs.

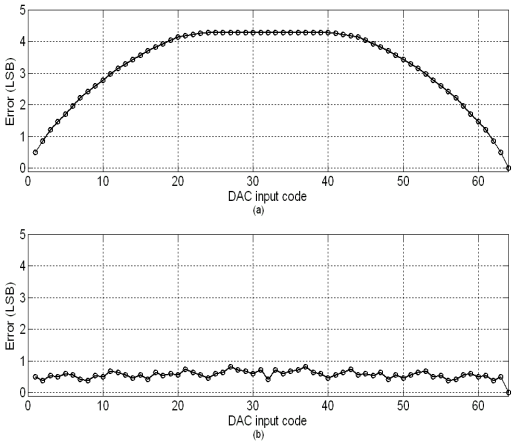


Fig. 6. The maximum output error of each DAC input code employing (a) randomization and (b) the RTC technique

III. ANALYSIS FOR RETURN-TO-ZERO CIRCUIT

Isolation transistors M_{i1} and M_{i2}, as shown in Fig. 7(a), cascoded to the drains of the switching transistors for the current cells of the DACs, can be used to decrease the coupling of the control signals to the output nodes [10]. However, these isolation transistors increase the output settling time and cause different rise and fall times [10]. Fig. 7(b) shows a simplified half-branch schematic of the current cell. For settling time analysis, if the gate state of M_2 is changed from low to high, the current through M_2 is switched off. The charge stored in the parasitic capacitor C_A is discharged to the output node through M_{i2}. The current through M_{i2} can be written as

$$I_{M_{i2}}(t) = K\left[\left(V_A(t) - V_{bias3}\right) - V_t\right]^2 \quad (1)$$

where $K=(\mu C_{ox}/2)(W/L)$ is the device transconductance parameter, $V_A(t)$ is the voltage of node A, V_{bias3} is the gate voltage of M_{i2}, and V_t is the threshold voltage of M_{i2}. The discharging current can also be written as

$$I_{M_{i2}}(t) = -\frac{dQ_A(t)}{dt} \quad (2)$$

where$Q_A(t)$ is the charge stored in node A. Equating (1) and (2), the equation of $V_A(t)$ can be derived as

$$V_A(t) = C_1 - \frac{ab\left(t + C_2\right) - 1}{b\left(t + C_2\right)} \quad (3)$$

where C_1 and C_2 are constants determined by initial conditions, $a=V_{bias3}+V_t$and $b=(K/C_A)$.Therefore, the settling time of the output nodes is increased due to the discharging behavior of node A.

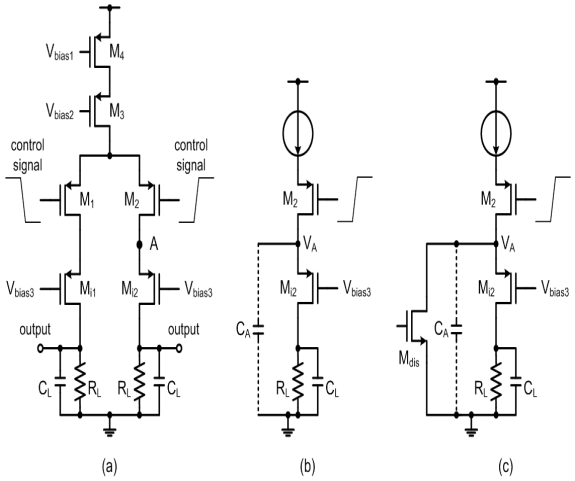


Fig. 7. (a) Current cell with isolation transistors, (b) its simplified half-branch schematic and (c) its simplified half-branch schematic with a discharging transistor

In order to overcome this problem, an extra discharging path can be added to node A as shown in Fig. 7(c). When M_{dis} is switched on, the charge stored in C_A is discharged immediatelyif $M_{dis}$is designed with high driving capability. Therefore, as shown in Fig. 8, the transistors M_{RTZ1} and M_{RTZ2} can alsodischargeinternal nodes and be used as RTZ transistors. When the RTZ control signal turns M_{RTZ1} and M_{RTZ2} on, the current from M_3 will flow through M_{RTZ1} or M_{RTZ2} according to the control signals of current switches M_1 and M_2. Therefore, the output voltages will settle to zero with a time constant of R_LC_L. Because the isolation transistors M_{i1} and M_{i2} are turned off, the signal dependent coupling of the control signals will be isolated during the RTZ period. Therefore, the RTZ circuit can achieve the properties of RTZ and isolation. For low-cost concerns, the RTZ transistors should be properly designed.

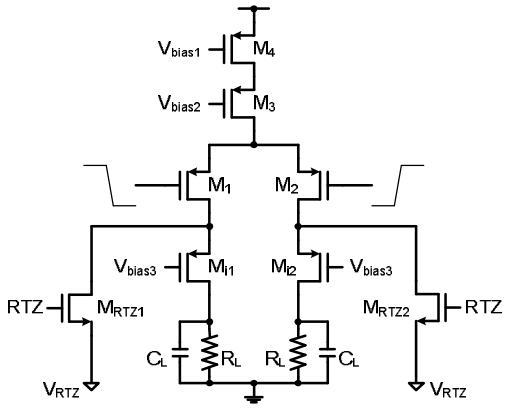


Fig. 8. Current cell with isolation and RTZ transistors

The RTZ transistors M_{RTZ1} and M_{RTZ2} can be either NMOS or PMOS. Considering the overdrive voltage and mobility for NMOS and PMOS, the size of the n-type RTZ transistor can be much smaller than that of the p-type RTZ transistor. Therefore, n-type RTZ transistors are used for the proposed low-cost DAC implementation.

IV. IMPLEMENTATION OF A 14-BIT CURRENT-STEERING DAC

A 14-bit current-steering DAC is implemented using the RTC, RTZ and HLS techniques. The design considerations of the DAC are presented as follows.

A. Segmentation and Matching Requirements of Current Cells

For the implementation of a low-cost current-steering DAC using the RTC technique, the DAC is segmented into the thermometer-code part and the binary-code part. For the thermometer-code part, the element mismatch effect is greatly reduced by using the RTC technique. For the 14-bit DAC, the DAC is segmented into six most significant bits (MSBs) and eight least significant bits (LSBs). For MSBs, the RTC technique and theproposed HLS for current sources are applied. Binary codes are used for LSBs. Monte-Carlo simulation results confirm that if current sources with 8-bit matching accuracy are adopted for the 14-bit DAC with the segmentation described above, the RTC technique can suppress harmonic distortions caused by mismatches to achieve SFDRs of over 80dB. To obtain a 99.7% yield for 8-bit matching accuracy using the equation derived in [14], the relative standard deviation of the LSB unit current can be obtained as

$$\frac{\sigma_{I_{LSB}}}{I_{LSB}} < \frac{1}{\sqrt{2^8}} \cdot \frac{0.5}{3.1} \approx 1\% \quad (4)$$

Using the mismatch model derived in [1], the area requirement for the LSB current-source transistors is

$$WL = \frac{\left[\frac{4A_{V_t}^2}{(V_{gs}-V_t)^2} + A_\beta^2\right] \cdot 0.5}{\frac{\sigma_{I_{LSB}}^2}{I_{LSB}^2}} \quad (5)$$

With a budget of 250mV for the overdrive voltage, the LSB current-source transistor has a dimension of 0.98μm/4.2μm.

The cascoded transistor is designed with a 200mV overdrive voltage. For reducing parasitic capacitance, the cascoded transistor has the same channel width as that of the current-source transistor. The current switches,the isolation transistors and the RTZ transistors use the minimum channel length for high operation speed and power saving.

B. Floorplan

The floorplan of the DAC is designed as follows. Current-source and cascoded transistors are placed together with buses connecting them to current switches. Latches, current switches, isolation transistors, and RTZ transistors are laid out apart from

the current-source and cascoded transistors to decrease the noise coupling from switching signals. Dummy transistors surround the current-source and cascoded transistors to suppress the edge effect.

C. Latch

The noises on the power supply lines can cause timing errors of the latches, which drive current switches of the DAC, and result in dynamic nonlinearity. To reduce the noises, the latch architecture with low transient current is used as shown in Fig. 9 [15]. In the latch circuit, transistors M_{N3} and M_{N4} offer extra driving capability of Vlatch to generate a low crossing point by causing different rise and fall times for the latch's differential outputs. Transmission gates TG_1 and TG_2 are adopted instead of switches with only one NMOS transistor. Buffers, B_1 and B_2, are added to suppress the clock-feedthrough from the transmission gates TG_1 and TG_2.

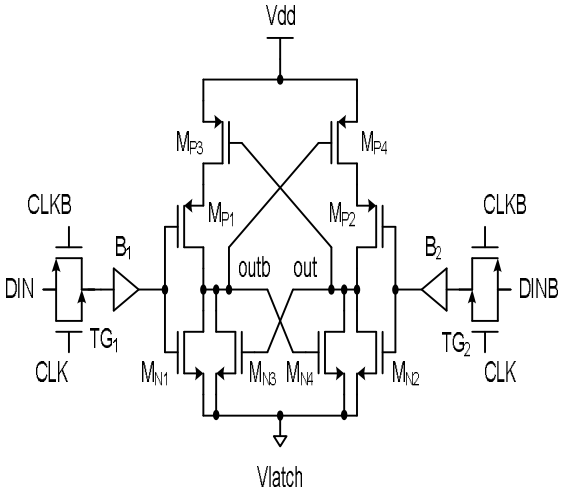


Fig. 9. Latch circuit

V. MEASUREMENT RESULTS

For the following measurement results, the RTC techniqueand the RTZ circuit are both enabled unless explicitly stated otherwise. Fig. 10 shows the DAC output spectrum for a 48.8MHz single-tone signal sampled at 100MHz. The measured SFDR is 80.85dB. Fig. 11 shows the single-tone SFDRs as a function of the input frequency for 4 different DAC configurations. For the DAC with both the RTC techniqueand the RTZ circuit enabled, the worst SFDR is 80.1dB. With the RTC technique enabled and the RTZ circuit disabled, the SFDR decreases rapidly when the input signal frequency is increased. With the RTC technique disabled and the RTZ circuit enabled, the SFDR values become less than 65dB, which is due to the use of small-area current sources. If the RTC technique and the RTZ circuit are both disabled, the SFDR values become much worse. Hence, the RTC techniqueand the RTZ circuit are very effective means to obtain high SFDR and high speed when small transistors with less matching are used.

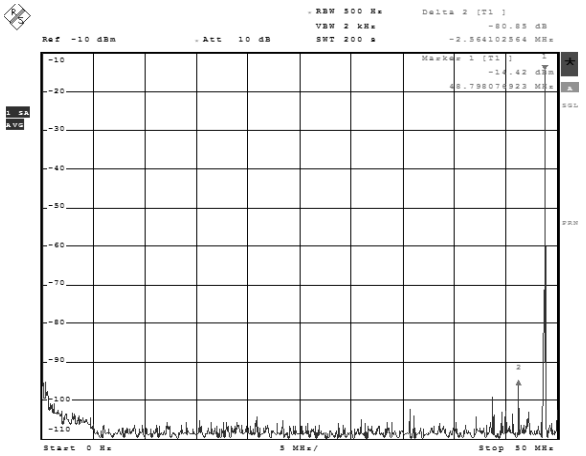


Fig. 10. Measured spectrum for a 48.8MHz signal at a 100MHz sampling frequency

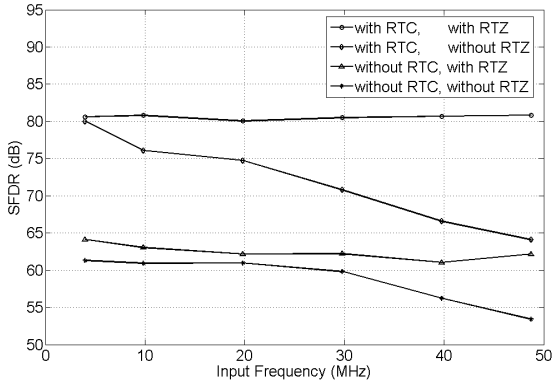


Fig. 11. SFDR versus input frequency for different configurations of the DAC at a 100MHz sampling frequency

The DAC was fabricated in a 0.18µm 1P6M process. Fig. 12 shows a photograph of the chip, which has an active area of less than 0.20mm^2. A comparison with recently published 14-bit DACs is given in Table I. Figure of merit (FoM) is usually used to evaluate the performance for analog-to-digital converters (ADCs). However, there is no well-recognized FoM equation for DACs. In addition to SFDR, clock frequency (f_{clk}) and total power consumption (P), the active area is also an important parameter used to evaluate the current-steering DACs. Therefore, the FoM given in (6)isadopted. As shown in Table I, the proposed DAC has the best FoM compared to recently published 14-bit DACs.

$$FoM = \frac{2^{\frac{SFDR_{Best}-1.76}{6.02}} \times 2^{\frac{SFDR_{Worst}-1.76}{6.02}} \times f_{clk}}{\left(P_{total} - \frac{1}{2} \times I_{load}^2 \times R_{load}\right) \times Area} \quad (6)$$

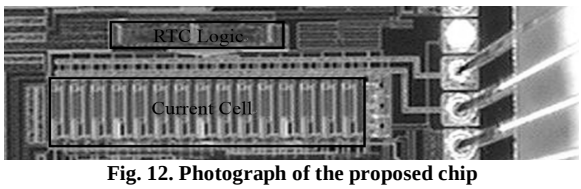


Fig. 12. Photograph of the proposed chip

Table I. Comparison of the proposed DAC with other 14-bit DACs

Specifications	This Work	[16]	[17]	[18]	[19]
Resolution, N	14	14	14	14	14
Process	0.18µm	0.18µm	0.13µm	0.18µm	0.14µm
Clock freq.(MHz)	100	500	500	3000	200
$SFDR_{Best}$ (dB)	80.8	83.7	84.8	84	84
$SFDR_{Worst}$ (dB)	80.1	68.9	73.5	52	78
I_{load} (mA)	10	10	16	20	20
Power (mW)	25	67.7	299	600	270
Active area (mm^2)	0.20	0.55	1.2	4	2.4
FoM (10^8MHz/mW*mm^2)	16.5	3.97	0.78	0.05	0.25

CONCLUSION

A current-steering DAC with the RTC,RTZ and HLS techniques has been implemented. It achieves high-speed and high-SFDR with a small active area. Further, the implemented DAC achieves the best FoM compared to other 14-bit DACs. However, this design was not focused on reducing power consumption. In addition, the design was targeted at 100MHz. Hence, more aggressive circuit design can further decrease the power consumption and increase the operation speed.

REFERENCES

[1] M. Pelgrom, A. Duinmaijer, and V. Welbers, "Matching properties of MOS transistors," IEEE J. Solid-State Circuits, vol. 24, no. 5, pp. 1433–1439, Oct. 1989.

[2] T.-H. Kuo, K.-D. Chen, and H.-R. Yeng, "A wideband CMOS sigma–delta modulator with incremental data weighted averaging," IEEE J. Solid-State Circuits, vol. 37, no. 1, pp. 11–17, Jan. 2002.

[3] K.-D. Chen and T.-H. Kuo, "An improved technique for reducing baseband tones in sigma–delta modulators employing data weighted averaging algorithm without adding dither," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 46, no. 1, pp. 63–68, Jan. 1999.

[4] D.-H. Lee and T.-H. Kuo, "Advancing data weighted averaging technique for multi-bit sigma–delta modulators," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 54, no. 10, pp. 838–842, Nov. 2007.

[5] D.-H. Lee, Y.-H. Lin, and T.-H. Kuo, "Nyquist-rate current-steering digital-to-analog converters with random multiple data-weighted averaging technique and Q^N rotated walk switching scheme," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 11, pp. 1264–1268, Nov. 2006.

[6] D.-H. Lee, T.-H. Kuo, and K.-L. Wen, "Low-cost 14-bit current-steering DAC with a randomizedthermometer-coding method," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 2, pp. 137–141, Feb. 2009.

[7] M.-H. Shen, J.-H. Tsai, and P.-C. Huang, "Random swapping dynamicelement matching technique for glitch energy minimization in current-steering DAC," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 5, pp. 369–373, May2010.

[8] P. Wang and N. Sun, "A random DEM technique with minimal element transition rate for high-speed DACs,"in Proc. IEEE ISCAS, 2014, pp. 1155-1158.

[9] A. R. Bugeja and B. Song, "A 14-b, 100-MS/s CMOS DAC designedfor spectral performance," IEEE J. Solid-State Circuits, vol. 34, no. 12,pp. 1719–1731, Dec. 1999.

[10] J. Vankka, J. Sommarek, J. Ketola, I. Teikari and K. A. I. Halonen, "A digital quadrature modulator with on-chip D/A converter," IEEE J. Solid-State Circuits, vol. 38, no. 10, pp. 1635-1642, Oct. 2003.

[11] D.-H. Lee and T.-H. Kuo, "Return-to-zero current-steering DAC with clock-to-output isolation," USA patent 7,576,675, Aug. 2009.

[12] I. Galton and P. Carbone, "A rigorous error analysis of D/A conversion with dynamic element matching," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 42, no. 12, pp. 763–772, Dec. 1995.

[13] Y. Cong and R. L. Geiger, "Switching sequence optimization for gradient error compensation in thermometer-decoded DAC arrays," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.,vol. 47, no. 7, pp. 585-595, July 2000.

[14] A. Van den Bosch, M. Steyaert, and W. Sansen, "An accurate statistical yield model for CMOS current-steering D/A converters," in Proc. IEEE ISCAS, 2000, pp. 105–108.

[15] K. O'Sullivan, C. Gorman, M. Hennessy and V. Callaghan, "A 12-bit 320-MSample/s current-steering CMOS D/A converter in 0.44mm^2," IEEE J. Solid-State Circuits, vol. 39, no. 7, pp. 1064-1072, July 2004.

[16] M. Liu, Z. Zhu and Y. Yang,"A High-SFDR 14-bit 500 MS/s Current-Steering D/A Converter in 0.18µm CMOS,"IEEE Transactions onVery Large Scale Integration (VLSI) Systems, vol. 23, no. 12, pp. 3148 - 3152, Dec. 2015.

[17] X. Li, "A 14 bit 500 MS/s CMOS DAC using complementary switched current sources and time-relaxed interleaving DRRZ," IEEE Trans. Circuits Syst. I, vol. 61, no. 8, pp. 2337-2347, Aug. 2014.

[18] G. Engel, S. Kuo and S. Rose, "A 14 b 3/6 GHz current-steeringRF DAC in 0.18µm CMOS with 66 dB ACLR at 2.9 GHz,"in Proc. IEEEISSCC, 2012, pp. 458–460.

[19] Y. Tang, "A 14 bit 200 MS/s DAC with SFDR >78 dBc, IM3 <−83 dBc and NSD <−163 dBm/Hz across the whole Nyquist band enabled by dynamic-mismatch mapping," IEEE J. Solid-State Circuits, vol. 46, no. 6, pp. 1371-1381, June 2011

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