A MULTI-OUTPUT STEP-UP/STEP-DOWN CONVERTER DESIGNED BY SWITCHED CAPACITOR TECHNIQUES

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Abstract- In this paper, a multi-output step-up/step-down DC-DC converter is designed by switched capacitor (SC) techniques. Unlike conventional multi-output SC converter such as a serial fix type converter, the proposed converter can offer stepped-up and stepped-down voltages without changing circuit topology. This paper also presents a novel analysis method to estimate properties of the multi-output converter. By assuming a five-terminal equivalent circuit, the proposed analysis method can derive the power efficiency and output voltages of multi-output converters without complex matrix calculations. The results of this study are as follows: (1) simulation program with integrated circuit emphasis (SPICE) simulations show that the proposed multi-output converter can improve power efficiency about 3% from the conventional serial fix type converter when the output load is 100Ω; and (2) the theoretical results are in good agreement with SPICE simulated results. The proposed analysis method is effective to estimate the power efficiency and output voltages of the multi-output SC converters.

Keywords- DC-DC Converters, Single-Input Multi-Output Converters, Step-Up/Step-Down Converters, Switched Capacitor Circuits.

I. INTRODUCTION

Recently, the market of mobile consumer products is growing rapidly, and many small and thin products are developed. Most of the mobile consumer products are powered by a lithium-ion battery, where some circuit units require different voltage levels. To provide multiple outputs at different voltage levels from a single DC supply, several DC power distributed systems have been used: low dropped regulator (LDO) arrays, single-input parallel-connected DC-DC converters, and so on. Among others, in order to reduce the number of external circuit components, multi-output DC-DC converters designed by switched-capacitor (SC) techniques have been proposed in recent years. The SC DC-DC converter can be realized without magnetic components. Therefore, the SC converter achieves not only small size but also small electromagnetic interference (EMI), though the conversion ratio of the SC converter is predetermined by its circuit topology. In previous studies, Suzukiet al. proposed a serial fix type DC-DC converter [1] designed by SC techniques.However, the serial fix type converter provides only the stepped-down voltages, V_{in}/N (N=1,2,3, …). Of course, as reported in [2], the conventional converter can generate stepped-up voltages by swapping the input and the output terminals. However,the serial fix type converter cannot control conversion ratios without changing circuit topology.Hua et al. suggested a single-input dual-output (SIDO) DC-DC converterfor energy harvesting applications [3]. By using a charge pump, the converter reported in [3] provides stepped-up voltages from a small DC supply, V_{in}. However, the conversion ratios of the conventional SIDO converter are only the stepped-up voltages, $N \times V_{in}$ (N=1,2,3, …). Chen et al. proposed an SC SIDO converter employing pseudo-three phase swap-and-cross control [4]. By connecting two series-parallel type converters [5] mutually, the conventional converter reported in [4] achieves step-up/step-down conversion without changing circuit topology. However, the circuit size becomes large, because two converters are necessary to achieve step-up/step-down conversion. Han et al. suggested a dual-output step up and down switched capacitor DC/DC converter [6]. By using three phase clock pulses, the conventional converter reported in [6] offers stepped-up and stepped-down voltages. However, the conventional converter reported in [6] can achieve only 8 gain pairs, because the circuit topology doesn't have a symmetry form.

In this paper, we propose a multi-output step-up/step-down DC-DC converter designed by SC techniques. Unlike conventional multi-output SC converter such as a serial fix type converter, the proposed converter can provide stepped-up and stepped-down voltages without changing circuit topology. This paper also presents a novel analysis method to estimate properties of the multi-output converters, because few studies have been done on the theoretical analysis of the multi-output SC converters. In the traditional theoretical analysis of SC DC-DC converters, the state-space averaging method has been commonly used [7]-[9]. However, the state-space averaging method requires complex matrix calculations.By assuming a five-terminal equivalent circuit, the proposed method can derive the power efficiency and output voltages without complex matrix calculations. To confirm the validity of the proposed converter, simulation program with integrated circuit emphasis (SPICE) simulations and theoretical analysis are performed.

The rest of this paper is organized as follows. In section 2, the circuit configuration of the proposed

converter is presented. In section 3, the property of the multi-output SC converter is analyzed by the proposed analysis method. Simulation results and experimental results are shown in Sections 4 and 5, respectively. Finally, conclusion and future work are drawn in section 6.

II. CIRCUIT CONFIGURATION

A. Conventional Converter

Fig. 1 shows an example of the conventional multi-output SC converter. The converter of Fig. 1 is based on the serial fix type converter proposed by Suzuki et al [1]. The conventional converter consists of six transistor switches and four capacitors, where transistor switches $S_{1,j}$, $S_{2,j}$, and $S_{3,j}$ (j=1, 2) are driven by non-overlapped three phase clock pulses. By controlling these transistor switches, the conventional converter offers the following stepped-down voltages:

$$V_{out1} = \left(\frac{1}{3}\right)V_{in} \quad \text{and} \quad V_{out2} = \left(\frac{2}{3}\right)V_{in}. \quad (1)$$

In the conventional converter, a fly-capacitor C_4 shuttles electric charge among the three voltage regions: $V_{in}/3$, $2V_{in}/3$ and V_{in}. Of course, by swapping the input and output terminals, the conventional converter can provide stepped-up and stepped-down voltages. Concretely, the conventional converter of Fig.1 can achieve 18 gain pairs: (V_{out1}, V_{out2}) = (V_{in}/3, $2V_{in}$/3), ($2V_{in}$/3,V_{in}), (V_{in}/3, V_{in}), ($2V_{in}$/3, V_{in}/3), (V_{in}, $2V_{in}$/3), (V_{in}, V_{in}/3), (V_{in}/2, V_{in}), (V_{in}, $3V_{in}$/2), (V_{in}/2, $3V_{in}$/2), (V_{in}, V_{in}/2), ($3V_{in}$/2, V_{in}), ($3V_{in}$/2, V_{in}/2), (V_{in}, $2V_{in}$), ($2V_{in}$, $3V_{in}$), (V_{in}, $3V_{in}$), ($2V_{in}$, V_{in}), ($3V_{in}$, $2V_{in}$), ($3V_{in}$, V_{in}). However,the conversion ratios of the conventional converter are predetermined by the circuit topology.For this reason, the application filed of the conventional converter is limited. Furthermore, the circuit control of the conventional converter is slightly complex, because the conventional converter requires threephase clock pulses to drive transistor switches. of course, by connecting extra fly-capacitors, the conventional converter can be controlled by two phase clock phases [2]. However, it is disadvantageous in hardware cost.

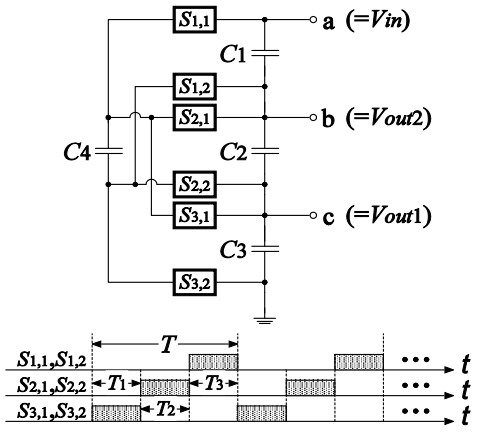
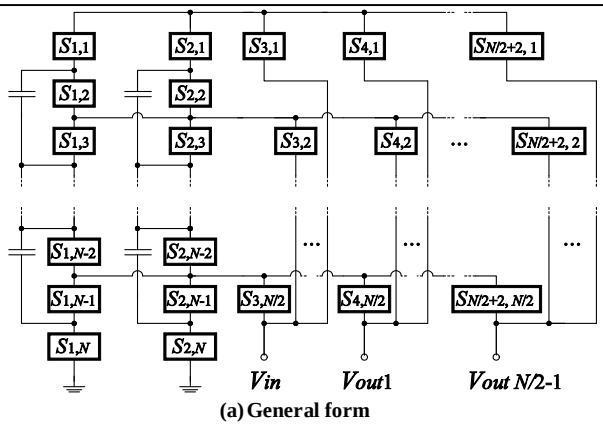
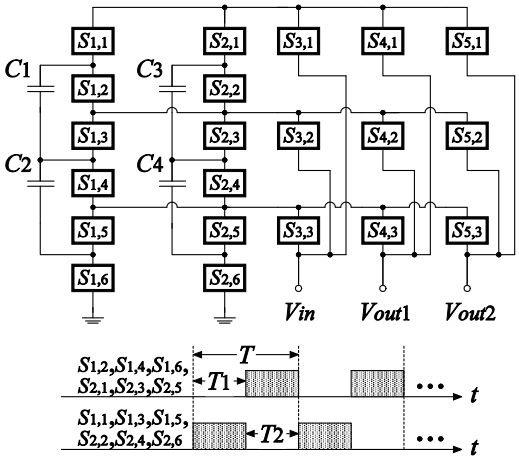


Fig. 1 Conventional dual-output SC DC-DC converter



(a) General form



(b) Simple example

Fig. 2 Proposed multi-output SC DC-DC converter

B. Proposed Converter

Fig. 2 shows the proposed multi-output SC converter. The proposed converter provides stepped-up and stepped-down voltages as follows:

$$V_{outi} = \left(\frac{s_i}{r}\right)V_{in}, \quad (2)$$

where $r, s_i = \{1, \ldots, N\}$ and $(i = 1, 2, \ldots, N/2 - 1)$.

For easy understanding, let's discuss the simplest example of the proposed converter shown in Fig. 2 (b). In Fig. 2 (b), the transistor switches$S_{1,j}$, $S_{2,j}$, and $S_{3,j}$ (j=1, …,6) are controlled by non-overlapped two phase pulses (see in Fig. 2 (b)), and$S_{3,n}$, $S_{4,n}$, and $S_{5,n}$ (n=1, 2,3)are transistor switches to swap the input and output terminals. According to the conversion ratios s_1/r and s_2/r(r, s_1, s_2={1, 2, 3}), one of the transistor switches $S_{m,n}$, (m=3, 4, 5) isturned on. In other words, by controlling $S_{3,n}$, $S_{4,n}$, and $S_{5,n}$, the conversion ratios s_1/r and s_2/r are determined. Concretely, the proposed converter of Fig. 2 (b) can offer the following 18 gain pairs:(V_{out1}, V_{out2}) = (V_{in}/3, $2V_{in}$/3), ($2V_{in}$/3,V_{in}), (V_{in}/3, V_{in}), ($2V_{in}$/3, V_{in}/3), (V_{in}, $2V_{in}$/3), (V_{in}, V_{in}/3), (V_{in}/2, V_{in}), (V_{in}, $3V_{in}$/2), (V_{in}/2, $3V_{in}$/2), (V_{in}, V_{in}/2), ($3V_{in}$/2, V_{in}), ($3V_{in}$/2, V_{in}/2), (V_{in}, $2V_{in}$), ($2V_{in}$, $3V_{in}$), (V_{in}, $3V_{in}$), ($2V_{in}$, V_{in}), ($3V_{in}$, $2V_{in}$), ($3V_{in}$, V_{in}). As (2) shows, the proposed converter of Fig.2 (b) can achieve

18 gain pairs without changing circuit topology. Furthermore, unlike the conventional converter of Fig.1, the proposed converter of Fig.2 requires only two phase clock pulses. However, the occupied silicon area of the proposed converter is bigger than that of the conventional converter of Fig.1. In the case of Fig.2 (b), the proposed converter requires 4 capacitors and 21 switches. On the other hand, 4 capacitors and 6 switches are necessary to design the conventional converter of Fig.1.

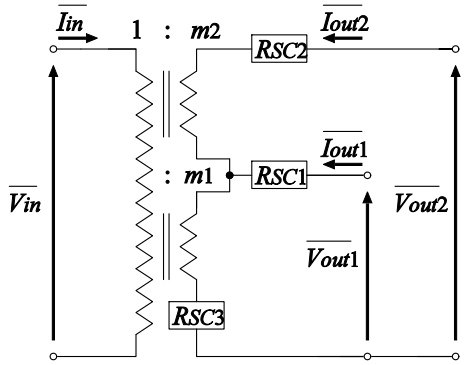
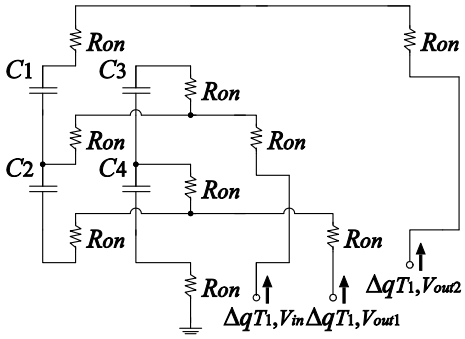
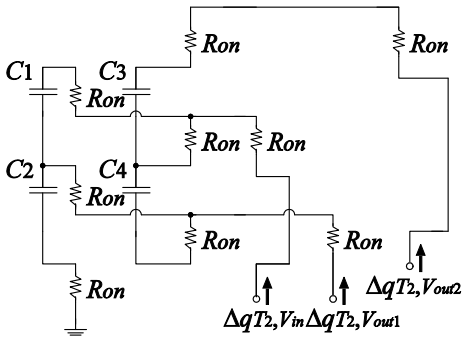


Fig. 3A five-terminal equivalent circuit



(a) State-T_1



(b) State-T_2

Fig. 4 Instantaneous equivalent circuits with conversion ratios of 1/2 and 3/2

III. THEORETICAL ANALYSIS

As an example, the property of the proposed converter is analyzed in conversion ratios of 1/2 and 3/2 theoretically. Unlike the traditional state-space averaging method, the proposed analysis method is performed by assuming a five-terminal equivalent circuit as shown in Fig. 3, because it is known that the general equivalent circuit of the single-input single-output SC DC-DC converter can be expressed as a four-terminal circuit [10], [11].In Fig. 3, R_{sc1}, R_{sc2}, and R_{sc3} are called the SC resistance and m_1 and m_2 are the conversion ratio of ideal transformers. The proposed analysis method derives these parameters from instantaneous equivalent circuits without complex matrix calculations.

Fig. 4 shows the instantaneous equivalent circuits of Fig. 2 (b). In Fig. 4, R_{on}denotes the on-resistance of the transistor switch. In the steady state, the differential value of electric charges in C_k (k=1, … , 4) satisfies the following equation:

$$\Delta q_{T_1}^{k} + \Delta q_{T_2}^{k} = 0 , \quad (3)$$

where Δq_{Ti}^{k} ((i=1, 2) and (k=1,…, 4)) denotes the electric charge of the k-th capacitor in the case of State-T_i. The interval of State-T_i satisfies the following conditions:

$$T = T_1 + T_2 \quad \text{and} \quad T_1 = T_2 = \frac{T}{2}, \quad (4)$$

where T is a period of the clock pulse and T_i (i=1, 2) is the interval of State-T_i.

In State-T_1, the differential values of electric charges in the input and the outputs, $\Delta q_{T1,Vin}$, $\Delta q_{T1,Vout1}$ and $\Delta q_{T1,Vout2}$, are obtained as

$$\Delta q_{T_1,V_{in}} = -\Delta q_{T_1}^{1} + \Delta q_{T_1}^{2} + \Delta q_{T_1}^{3},$$
$$\Delta q_{T_1,V_{out1}} = -\Delta q_{T_1}^{2} + \Delta q_{T_1}^{4} - \Delta q_{T_1}^{3},$$
$$\text{and} \quad \Delta q_{T_1,V_{out2}} = \Delta q_{T_1}^{1}. \quad (5)$$

On the other hand, in State-T_2, the differential values of electric charges in V_{in}, V_{out1} and V_{out2}, $\Delta q_{T2,Vin}$, $\Delta q_{T2,Vout1}$ and $\Delta q_{T2,Vout2}$, are obtained as

$$\Delta q_{T_2,V_{in}} = \Delta q_{T_2}^{1} - \Delta q_{T_2}^{3} + \Delta q_{T_2}^{4},$$
$$\Delta q_{T_2,V_{out1}} = -\Delta q_{T_2}^{1} + \Delta q_{T_2}^{2} - \Delta q_{T_2}^{4},$$
$$\text{and} \quad \Delta q_{T_2,V_{out2}} = \Delta q_{T_2}^{3}. \quad (6)$$

In (5) and (6), the following conditions are satisfied, because the instantaneous equivalent circuits have symmetrical structure as shown in Fig. 4.

$$\Delta q_{T_1}^{1} = \Delta q_{T_2}^{3}, \quad (7)$$
$$\Delta q_{T_1}^{2} = \Delta q_{T_2}^{4},$$
$$\Delta q_{T_1}^{3} = \Delta q_{T_2}^{1},$$
$$\text{and} \quad \Delta q_{T_1}^{4} = \Delta q_{T_2}^{2}.$$

Using (5) and (6), the average input current and the average output currents can be expressed as

$$\overline{I_{in}} = \frac{\Delta q_{V_{in}}}{T} = \frac{\Delta q_{T_1,V_{in}} + \Delta q_{T_2,V_{in}}}{T},$$
$$\overline{I_{out1}} = \frac{\Delta q_{V_{out1}}}{T} = \frac{\Delta q_{T_1,V_{out1}} + \Delta q_{T_2,V_{out1}}}{T},$$

and $$\overline{I_{out2}} = \frac{\Delta q_{V_{out2}}}{T} = \frac{\Delta q_{T_1,V_{out2}} + \Delta q_{T_2,V_{out2}}}{T}. \quad 8)$$

In (8), Δq_{Vin}, Δq_{Vout1}, and Δq_{Vout2} are electric charges in V_{in}, V_{out1}, and V_{out2}, respectively. Substituting (3)-(7) into (8), we have the relation between the average input current and the average output currents as follows:

$$\overline{I_{in}} = -\frac{1}{2}\overline{I_{out1}} - \frac{3}{2}\overline{I_{out2}}. \quad (9)$$

From (9), the conversion ratios in Fig. 3 are obtained as m_1=0.5 and m_2=1.

Next, in order to derive the SC resistances R_{SC1}, R_{SC2}, and R_{SC3}, the consumed energy in one period is discussed. From Fig. 4(a), the consumed energy W_T can be expressed as

$$W_T = W_{T_1} + W_{T_2} = 2W_{T_1}, \quad (10)$$

where

$$W_{T_1} = \frac{\left(\Delta q_{T_1}^4\right)^2}{T_1} R_{on} + \frac{\left(\Delta q_{T_1,V_{out2}}\right)^2}{T_1} R_{on} + \frac{\left(\Delta q_{T_1}^2\right)^2}{T_1} R_{on} + \frac{\left(\Delta q_{T_1}^1 - \Delta q_{T_1}^2\right)^2}{T_1} R_{on} + \frac{\left(\Delta q_{T_1}^3\right)^2}{T_1} R_{on} + \frac{\left(\Delta q_{T_1}^3 - \Delta q_{T_1}^4\right)^2}{T_1} R_{on} + \frac{\left(\Delta q_{T_1,V_{in}}\right)^2}{T_1} R_{on} + \frac{\left(\Delta q_{T_1,V_{out1}}\right)^2}{T_1} R_{on}.$$

Using (3)-(7), the consumed energy (10) is rewritten as

$$W_T = \frac{9\left(\Delta q_{V_{out1}}\right)^2}{4T} R_{on} + \frac{25\left(\Delta q_{V_{out2}}\right)^2}{4T} R_{on} + \frac{6\left(\Delta q_{V_{out1}} \cdot \Delta q_{V_{out2}}\right)}{4T} R_{on}. \quad (11)$$

Here, the consumed energy W_T of the five-terminal equivalent circuit shown in Fig. 3 is obtained as

$$W_T = R_{SC1}\left(\overline{I_{out1}}\right)^2 T + R_{SC2}\left(\overline{I_{out2}}\right)^2 T + R_{SC3}\left(\overline{I_{out1}} + \overline{I_{out2}}\right)^2 T$$

$$= \left(R_{SC1} + R_{SC3}\right)\frac{\left(\Delta q_{V_{out1}}\right)^2}{T} + \left(R_{SC2} + R_{SC3}\right)\frac{\left(\Delta q_{V_{out2}}\right)^2}{T} + 2R_{SC3}\frac{\left(\Delta q_{V_{out1}} \cdot \Delta q_{V_{out2}}\right)}{T} \quad (12)$$

.

Therefore, from (11) and (12), we have the SC resistances as follows:

$$R_{SC1} = \frac{3}{2}R_{on},$$

$$R_{SC2} = \frac{11}{2}R_{on},$$

and $$R_{SC3} = \frac{3}{4}R_{on}. \quad (13)$$

By combining (9) and (13), the parameters in Fig. 3 are obtained as m_1=0.5, m_2=1, R_{SC1}=(3/2)R_{on}, R_{SC2}=(11/2)R_{on}, and R_{SC3}=(3/4)R_{on}. Therefore, the power efficiency and the output voltages can be derived from the equivalent circuit of Fig. 3. Using a principle of superposition, we have the output voltages V_{out1} and V_{out2} as follows:

$$V_{out1} = V_{out1,1} + V_{out2,1}, \quad (14)$$

where $$V_{out1,1} = \frac{\left(V_{in}/2 - V_{x1}\right)R_{L1}}{R_{SC1} + R_{L1}},$$

$$V_{out2,1} = \frac{\left(V_{in}/2 - V_{x1}\right)R_{L2}}{R_{SC2} + R_{L2}},$$

and $$V_{x1} = \frac{\left(V_{in}/2\right)R_{SC3}}{R_{SC3} + \left(R_{SC1} + R_{L1}\right)//\left(R_{SC2} + R_{L2}\right.}$$

and

$$V_{out2} = V_{out1,2} + V_{out2,2}, \quad (15)$$

where $$V_{out1,2} = \frac{-V_{x2}R_{L1}}{R_{SC1} + R_{L1}},$$

$$V_{out2,2} = \frac{\left(V_{in} - V_{x2}\right)R_{L2}}{R_{SC2} + R_{L2}},$$

and $$V_{x2} = \frac{\left\{\left(R_{SC1} + R_{L1}\right)// R_{SC3}\right\}V_{in}}{\left(R_{SC2} + R_{L2}\right) + \left(R_{SC1} + R_{L1}\right)// R_{SC3}}$$

In (14) and (15),R_{L1} and R_{L2} are output loads.Furthermore, the power efficiency η of the proposed converter can be derived as

$$\eta = \frac{R_{L1} + R_{L2}\alpha^2}{\left(R_{SC1} + R_{L1}\right) + \left(R_{SC2} + R_{L2}\right)\alpha^2 + R_{SC3}\left(1 + \alpha\right)^2} \quad (16)$$

,

where $\alpha = \dfrac{3\left(R_{SC1} + R_{L1}\right) + 2R_{SC3}}{R_{SC2} - 2R_{SC3} + R_{L2}}$.

IV. SIMULATION

In SPICE simulations, the property of the proposed converter is compared with that of the conventional converter shown in Fig. 1. The SPICE simulations are performed under conditions that V_{in} = 3.7V, $C_1 = C_2 = C_3 = C_{out1} = C_{out2}$ = 1μF, R_{on} = 1Ω, T_i = 0.5μs and $R_L=R_{L1}=R_{L2}$, where C_{out1} and C_{out2} are output capacitors connected to the output terminals.

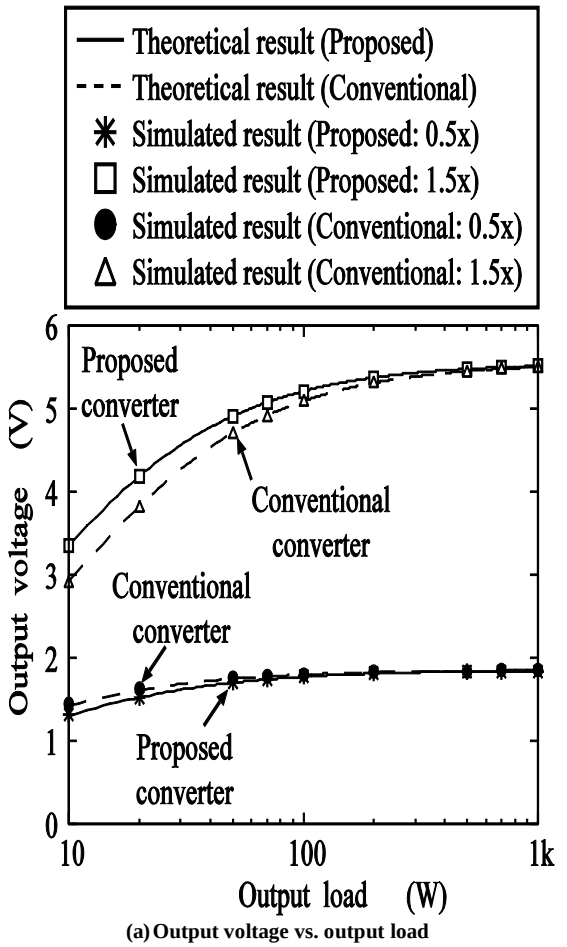
Fig.5 shows the comparison of the simulated output voltages between the proposed converter and the conventional converter of Fig. 1. As Fig.5 shows, the

proposed converter can provide stepped-up and stepped-down voltages without changing circuit topology. To realize the conversion ratios of 1/2 and 3/2, the clock pulses for the proposed converter and the conventional converter were set to as shown in Tables 1 and 2.

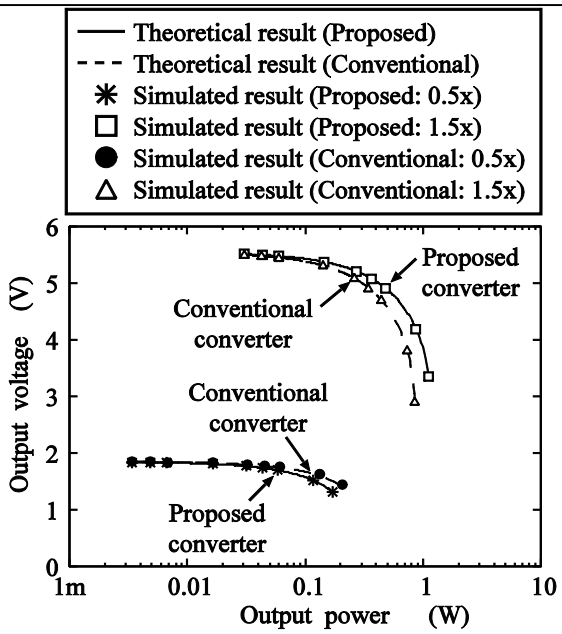
In the conventional converter, the input terminal V_{in} and the output terminals V_{out1} and V_{out2} are set to the terminal b, a, and c, respectively.(see Fig. 1.) In Fig.5, the solid lines show the theoretical results obtained by (14) and (15). As Fig.5 shows, the theoretical results are in good agreement with the simulated results.

Fig. 6 shows the simulated efficiency with conversion ratios of 1/2 and 3/2. In Fig. 6, the solid lines show the theoretical results obtained by (16). As Fig. 6 shows, theoretical results agree well with SPICE simulated results. From Figs. 5 and 6, the validity of the theoretical analysis can be confirmed.

The derived theoretical equations will be helpful to estimate the properties of the proposed converter. Furthermore, as Fig. 6 shows, the proposed converter can improve the power efficiency about 3% from the conventional converter when the output load is 100Ω. The proposed converter can achieve more than 75% efficiency over a range of output power from 0.1W to 1W.



(a) Output voltage vs. output load



(b) Output voltage vs. output power

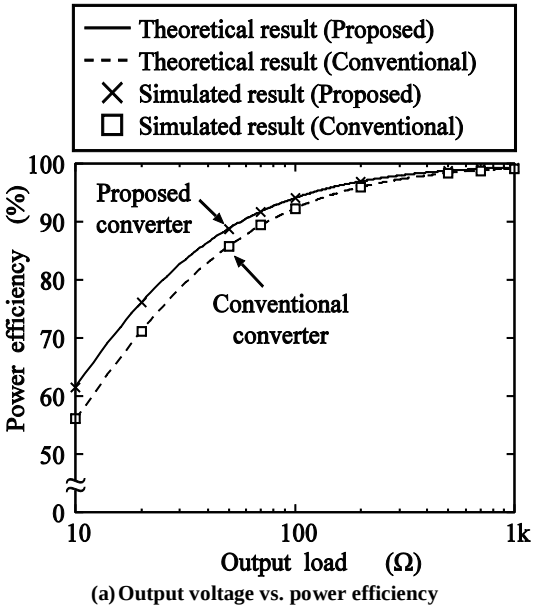
Fig. 5 Simulated output voltage

TABLE I
TIMING OF CLOCK PULSES FOR THE PROPOSED CONVERTER

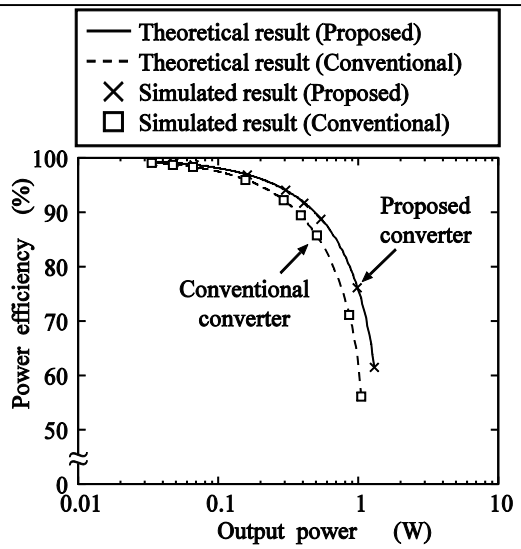
State	On	Off
T_1	$S_{1,1}$, $S_{1,3}$, $S_{1,5}$, $S_{2,2}$, $S_{2,4}$, $S_{2,6}$, $S_{3,2}$, $S_{4,3}$, $S_{5,1}$	Others
T_2	$S_{1,2}$, $S_{1,4}$, $S_{1,6}$, $S_{2,1}$, $S_{2,3}$, $S_{2,5}$, $S_{3,2}$, $S_{4,3}$, $S_{5,1}$	Others

TABLE III
TIMING OF CLOCK PULSES FOR THE CONVENTIONAL CONVERTER

State	On	Off
T_1	$S_{1,1}$, $S_{1,2}$	Others
T_2	$S_{2,1}$, $S_{2,2}$	Others
T_3	$S_{3,1}$, $S_{3,2}$	Others



(a) Output voltage vs. power efficiency



(b)Output voltage vs. power efficiency

Fig. 6 Simulated power efficiency

V. EXPERIMENT

Fig.7 shows the photograph of the experimental circuit. The experimental circuit of Fig. 7 was built with commercially available ICs AQV212 and TD62004APG on a bread board, where V_{in} = 3.7V, C_1 = C_2 = C_3 = C_{out1} = C_{out2} = 10μF, T=1ms and R_{L1}=R_{L2}=10kΩ. In the experiments, we focused on the verification of the circuit topology, because the experimental circuit was built with commercially available ICs on a bread board.

Fig. 8 shows the measured output voltages of the proposed converter, where the 1/2x and 3/2x conversion ratios are realized. In Fig.8, the measured output voltages are 1.81V and 5.54V, where the ideal outputs are 1.85V and 5.55. Fig. 9 shows the measured output voltages with conversion ratios of 1/3 and 2/3. In Fig. 9, the measured output voltages are 1.23V and 2.46V, where the ideal outputs are 1.17V and 2.45. As Figs.8 and 9 shows, the proposed converter can control conversion ratios without changing circuit topology. Furthermore, the validity of the proposed topology can be confirmed byFigs.8 and 9.

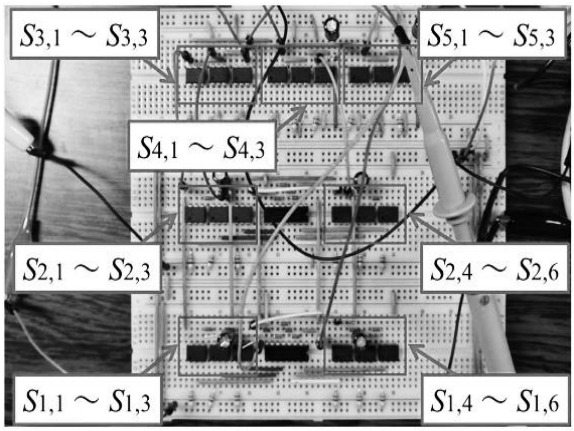


Fig. 8Experimental circuit

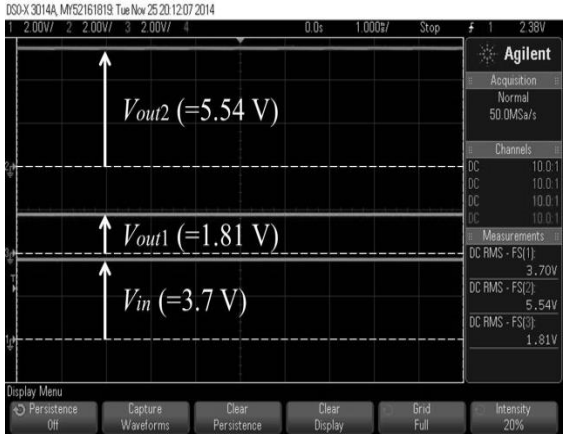


Fig. 9Measured output voltages with conversion ratios of 1/2 and 3/2

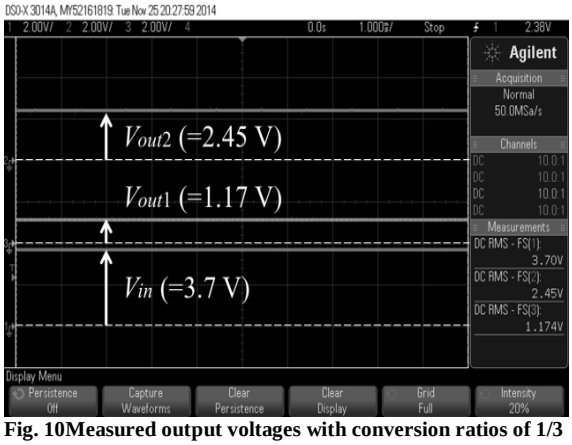


Fig. 10Measured output voltages with conversion ratios of 1/3 and 2/3

CONCLUSION

A multi-output SC converter and its analysis method have been proposed in this paper. The results of this study are as follows: (1) unlike the serial fix type converter, not only a stepped-down voltage but also a stepped-up voltage was offered by the proposed converter without changing circuit topology; (2) the proposed converter improved power efficiency about 3% from the serial fix type converter when the output load was 100Ω; and (3) handy theoretical equations to estimate properties of the multi-output converter were obtained without complex matrix calculation. The theoretical results were in good agreement with simulated results. The detailed experiment of the proposed converter is left to a future study.

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