A5.8 GHZ FRACTIONAL-N SYNTHESIZER FOR WIRELESS TRANSCEIVER APPLICATIONS

YAN DAN LEI,[1]ZHAO BIN, YOSHIDA AKIRA, KASA YASUSHI, M. KUMARASAMY RAJA

Institute of Microelectronics, A*STAR, Singapore
CM Engineering Co., Ltd, Japan
E-mail: yandl@ime.a-star.edu.sg

Abstract - This paperpresents a 5.8 GHz fractional-N synthesizer that is used for wireless transceiver applications in 55nm CMOS process. The synthesizer could cover 5.8GHz frequency band with quadrature I/Q output. Simulations show that the phase noise (PN)@11.6GHzof the synthesizer is -80dBc/Hz, -95dBc/Hz and -105dBc/Hz with frequency offsets of 50kHz, 100kHz and 1MHz respectively. The die area of the proposed synthesizer is 0.6mm X 0.7mm. Thecurrent consumption of the synthesizer is 15mA with 1.2V supply voltage.

Keywords - CMOS, PLL, FRACTIONAL-N Synthesizer

I. INTRODUCTION

Wireless communication is widely used in modern life, from the few MHz near field wireless detector sensor to 4G mobile, Bluetooth, WLAN to Terahertz radar application.The core wireless communication is the data transmission through the different frequency range Electromagnetic wave radiation. Ina wireless communication system, two-way radio that combines both a radio transmitter and a receiveris named transceiver.

The physical layer of communication systemis mainly the transceiveras in [1] that is a combination transmitter/receiver in a single package for short-range communication. The frequency synthesizers are used to generate the high stability and accuracy signal for transceiver application. This paper presents a 5.8GHz fractional-N synthesizer for wireless communicationapplication in 55nm CMOS process. The synthesizer could cover 5.8GHz frequency band with quadrature I/Q output. Simulations show that the phase noise at the frequency of 11.6GHz of the synthesizer is -80dBc/Hz, -95dBc/Hz and -105dBc/Hz with frequency offsets of 50kHz, 400kHz and 1MHz respectively.

The die area of the proposed synthesizer is 0.6mm X 0.7mm. The following will be describedin this paper. In part2, the architecture of fractional-N synthesizer is introduced and the key building blocks of synthesizer are explained in detail. Meanwhile, designchallenges and topologies are introduced also. The layout and chip implementation are also briefly explained. In part 3, the results of simulation are discussed.

II. ARCHITECTURE

The block diagram of fractional-N synthesizer is shown in the Fig.1.The synthesizer use 10 to 24MHz crystal oscillator as the reference signal.The doubler is used to generate 2 times reference frequency, in order to reduce the synthesizer's in-bandphase noise.

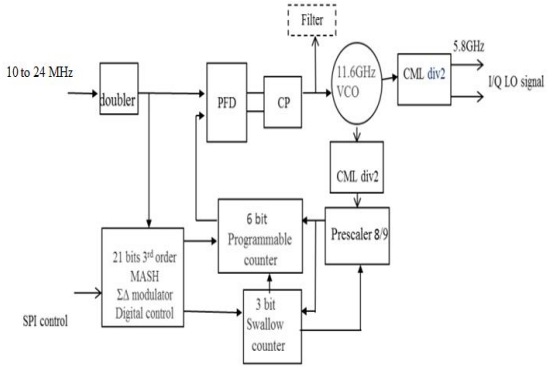


Fig 1: The fractional-N synthesizer's block diagram

The synthesizer consists of a 11.6GHz LC voltage controlled oscillator(VCO), a current mode logic (CML) divide by 2 counter, a true single phase clock (TSPC) prescaler 8/9, a charge-pump (CP) and a phase frequency detector (PFD), a 6 bits programmable counter,3 bits swallow counter and a 21 bits delta-sigma (DS) 3rd order MASH modulator with digital control circuit. The 11.6GHz signal will be divide by 2 to generate quadrature 5.8GHz I/Q signals to be fed to the mixers in transmitter and receiver.

2.1. Voltage Controlled Oscillator (VCO)

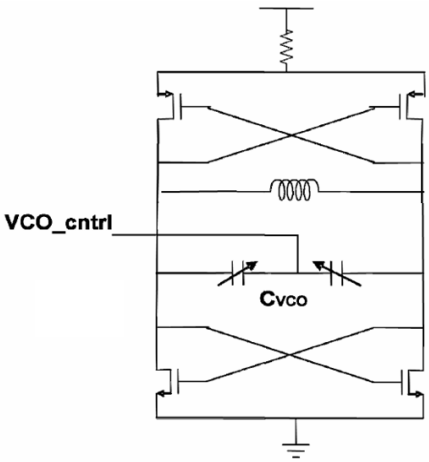


Fig 2: The circuit diagram of 11.6GHz VCO

In order to meet accurate I-Q generation performance in the synthesizer, an 11.6GHzLCVCO [2], operating at twice the RF frequency, is used as shown in Fig.2. For the sake of lower phase noise for LC oscillator ispreferred over ring oscillators in CMOS process. The VCO uses a cross-coupled complimentary MOS as active devices.In order to reduce the close-in phase noise, the VCO uses a resistive current bias to reduce the phase noise from few hundred Hz to few hundred KHz offset. A high-Q,singleturn symmetrical top-metal octagonal inductor is used to achieve lower phase noise.

2.2. PFD and CP

A phase frequency detector(PFD)is used to detect the frequency and phase error of PLL. PFD together with charge pump (CP) exhibits unlimited locking range and can be easily implemented in CMOS process. In this design, the phase frequency detector is dead-zone free, which means that UP and DOWN(DN) control signal turn on together when PLL is locked, in order to improve the reference spur and in-band phase noise of thesynthesizer.

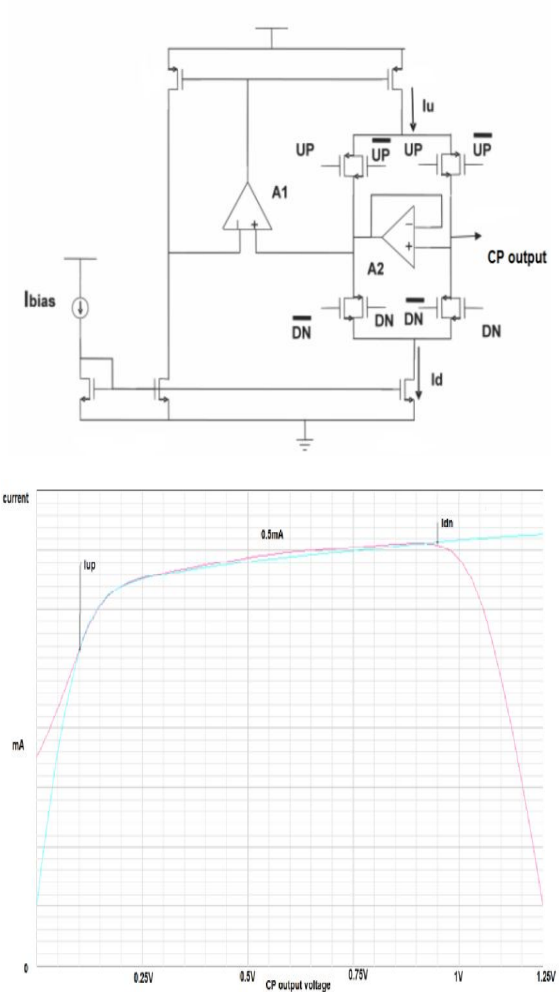


Fig 4: The simulation result of charge pump current mismatch

In a fractional-N synthesizer, the current mismatch of charge pump affects the in-band phase noise and reference spur. In this design, a charge pump circuit as shown in Fig.3, employsthe feedback operational amplifier A1 is used to make sure Iu and Id are equal. Switched transistors are controlled by UP and DN signals from PFD, The Iu and Id current is turned on/off to charge and discharge the CP output node. The size of transistors are optimized to reduce the mismatch current and to increase the CP output impedance. TheFig.4shows the simulatedmismatch of Iu and Id andis less than 3% when the output voltage of CP vary from 0.3 to 0.9V.

2.3 Divder, Counter and Digital circuit

The high speed divider includes an11.6GHz current mode logic(CML) divide by 2counter and a true single phase(TSPC) prescaler 8/9 counter [3], 6 bits programmable (P) counter and 3 bits swallow (S) counter. Total counter value is 2*(8P+S), (P, S is the register value of programmable and swallow counter).

CML divider achieves high-speed operation by lowering output voltage swing compared to the static CMOS circuits with small area. Fig.5. shows the schematic of 11.6GHz divide by 2 counter, the counter includes a master CML D latch (M latch)and a slave CML D latch (S latch) with the output of M latchinversely connected to the input of S latch. The CML D latch uses the poly resistors as loads.

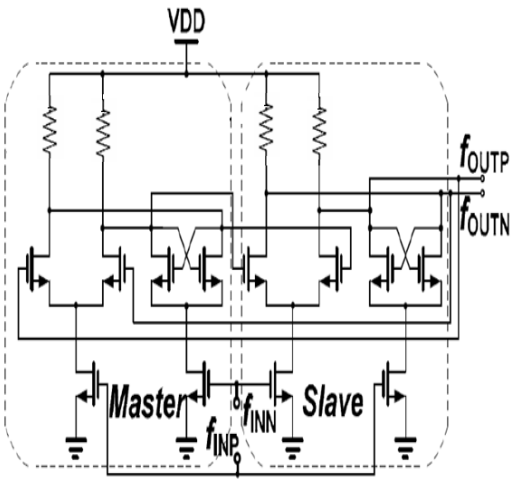


Fig 5: The block diagram of CML divides by 2

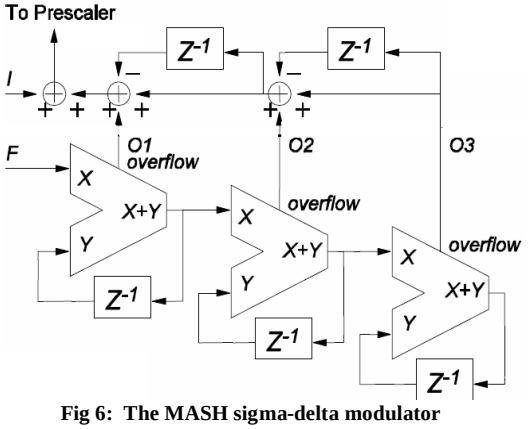


Fig 6: The MASH sigma-delta modulator

The P, S counter is controlled by the 21-bit 3rd order MASHDS modulator. The overflow of modulator is then added to the P/S counter to generate the fractional-N counter value. The MASH modulator is shown as follows in Fig.6.

2.4 Layout and Implementation

The Layout of fractional-N synthesizer is shown in Fig.7. In order to reduce noise coupling and spur, layout was carefully planned. All the digital circuits, i.e. PFD, divider counters and DS modulator, are clocked by reference frequency, and hence can potentially generate reference noise. The reference noise will then generate reference spur at the output of the synthesizer. In order to reduce this digital noise coupling, all of above digital circuit are drawn with additional guard ring and shielding. At same time, in order to eliminate the digital noise coupled to VCO and analog circuit through power supply and ground, the digital and analog power supply and ground are separated.

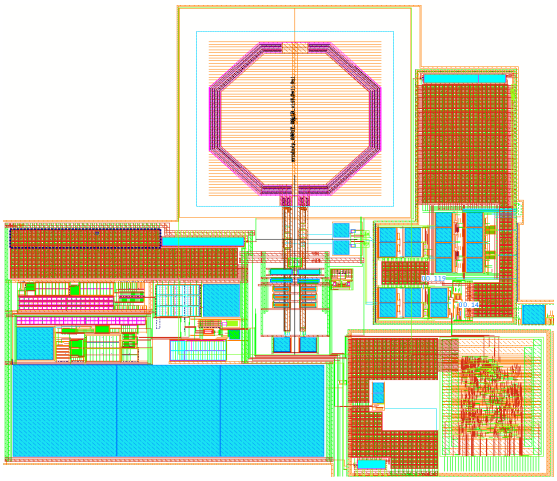


Fig 7: Layoutof fractional-N synthesizer

The VCO inductor layout occupies large area and is susceptible to electromagnetic coupling. So a thick guard ring and shielding is added to the inductor. In the test PCB, there are enough de-coupling caps between separated power supply and ground.

III. RESULTS AND DISCUSSION

The fractional-N synthesizer is designed and implemented in 55nm standard CMOS process with RF option. The layout area is 0.6mm × 0.7mm. The simulated phase noise in synthesizer levelis -80dBc/Hz@11.6GHz, -95dBc/Hz and -105dBc/Hz with offsets of 50kHz,400kHz and 1MHz offset respectively at 5.83GHz as shown in Fig.8. The synthesizer loop bandwidth is about200 kHz. Integrated jitter is 1.6 degree from 10 kHz to 6MHz. The current consumption of each blocks are shown is Table I

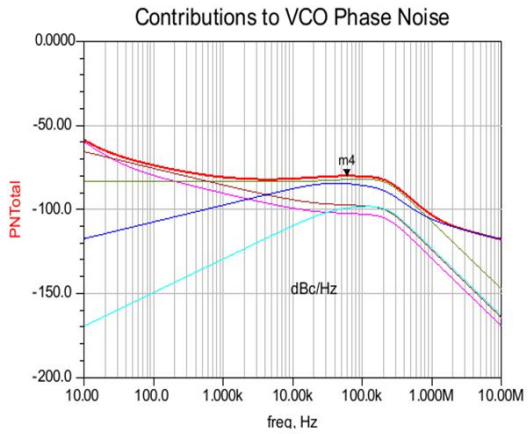


Fig8: Phase noise of fractional-N synthesizer @ 11.6GHz

Table 1 Current consumption for each synthesizer block

Block	mA
VCO and buffer	6.5
Div by 2 for I/Q LO and buffer	3
Prescaler8/9	1.5
PFD & CP	2.5
P/S counter, Σ-Δ modulator programmable counter	1.5
Total	15

This paper described thedesign, layout and implementation of fractional-N synthesizer. The operation of the synthesizer is evaluated by post layout simulation of 55-nm CMOS technology. The synthesizer is proven to be useful in a wireless transceiver system.

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