LOW-POWER DIGITAL CONTROL UNIT FOR MULTI-CHANNEL IMPLANTABLE NEUROMUSCULAR CURRENT STIMULATOR

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Abstract – This paper proposes a robust and flexible controller for multi-channel neuromuscular current stimulator chip. The design supports various modes of operations, including housekeeping modes, debugging modes and finally stimulation control modes. For debugging, it is able to monitor internal operating nodes and long-term data transmission bit error rates. For simulation control, it is capable of storing pre-defined stimulation patterns and controls eight individual channels simultaneously. The design was implemented and verified using standard 0.18 um/ 1.8 V CMOS process. Finally it was integrated in a neuromuscular SoC with completed analog front-end and wireless power harvesting circuit.

I. INTRODUCTION

Fully implantable electronic that can record electroneurogram (ENG) signal and provides necessary electrical stimulations to the peripheral nerves is a promising approach to restore functions of nerve injuries[1]. To provide practical, long-term implantable solutions to injured patients, IC chips that are responsible for weak ENG signal recording and peripheral nerve stimulations must be reliable, consume low-power and have small form factors[2].
Several neural acquisition and stimulation systems have been reported to date [1, 3-15]. These devices are powered by either on-chip inductive power coupling or on-board battery forsignal processing, analog-front end stimulation and data telemetry. However, these prototypes still have large form factor due to theuse of large or multiple off-the-shelf components that inhibit further size reduction. Furthermore, most of them do not have a versatile and flexible programmable central control that can truly support long-term, easy to use stimulation set-up. For example in [15], the core analog front-end, the digital feedback and the DAC were implemented off-chip but the ADC and global control were off-chip. In [7] the core stimulator circuit was implemented without smart global control. It is not able to store any pre-defined pattern or perform any self-debug capabilities. Similarly, in [9], three separated board are needed to perform stimulation on a rat. Even thought, its practical use is limited, not because of the stimulation front-end but the lack of a compact and versatile digital control. To overcome limitations of the existing works, we propose a low-power, robust digital control unit that can support multiple modes of operations: Housekeeping, debugging and flexible stimulation set-up. It also allow users to store multiple pre-defined stimulation sequences that can be called arbitrarily within one stimulation session. The paper is organized as follows: The SoC architecture isintroduced in Section II. The design's operating principle and implementation are discussed in Section III and IV, respectively. Section V concludes the paper.

II. DESIGN OVERVIEW: PROCESSOR FOR MULTI-CHANNEL NEUROMUSCULAR CURRENT STIMULATOR

Our implantable multi-channel current simulation SoC (Fig. 1) consists of an inductive power harvesting circuit, on-chip clock and data recovery circuit, 8-channel differential bi-phasic neuromuscular current stimulator front-end, an internal relaxation oscillator, a data modulator that serves to transmit the packaged data coming from digital core, and finally a central digital control logic (DCL).

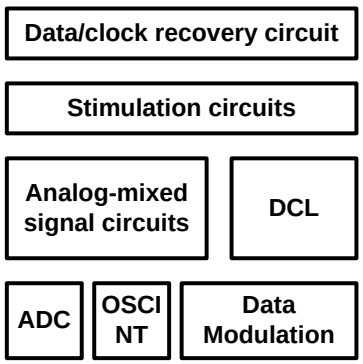


Fig. 1 The main functional units of the proposed SoC.

To ensure long-term, reliable operation of the implantable ICs as well as to support extensive electrical testing and characterization, our design was implemented with the capability to handle multiple modes of operations, depending on the external commands. More specifically, it is responsible for:

- Decode the commands, stimulation triggers and stimulation programs (in UART format) that are received from the high voltage inductive powered clock and data recovery unit and deliver the control bits (in JTAG format) to the various control registers to various blocks in the design.

- Establish the stimulation sequence control of stimulation front end according to stimulation commands coming from theexternal master.
- Establish the oscillator frequency tuning mode and facilitate frequency tuning via the JTAG registers.
- Establish the analog signal probing for operating point debugging of the analog blocks.
- Among these operation, establishing stimulation sequence control is the most complex and important mode for the stimulation circuit. Its block diagram in shown in Fig. 2.

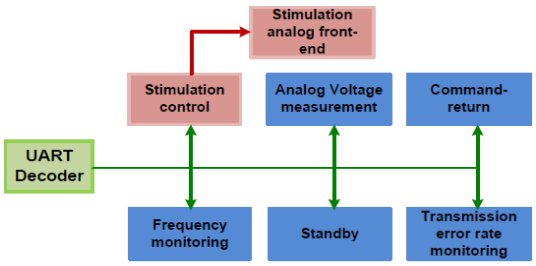


Fig. 2. Simplified digital control block diagram

Our design communicates with external devices using UART protocol, as shown in Fig. 3. Each UART frame has a start bit (zero), followed by 7 message bits, a parity bit and ends with a stop bit (one). During standby, the UART data line is maintained high (i.e. 1). A UART decoder is used to accept various supported commands and subsequently activate the corresponding blocks to perform the necessary actions. The general format of the incoming UART commands that are sent to the control unit would have the format show in Fig. 4. To ensure correct package transmission synchronization, repeated frames with the same data are sent to the chip prior to any actual OpCode. In this implementation, five "A5" frames are used, followed by a SYNC frame "EF". The 7th frame contains the actual OpCode, followed by various specific control data. The length of the control data depends on the OpCode and thus must be handled carefully. Finally, a synchronization frame "5A" is sent to indicate the end of the OpCode transmission.

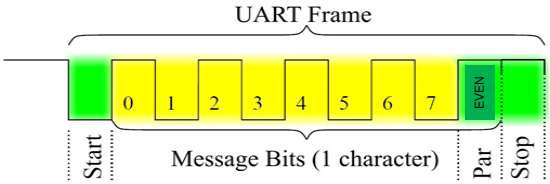


Fig. 3 A single UART frame that would be received

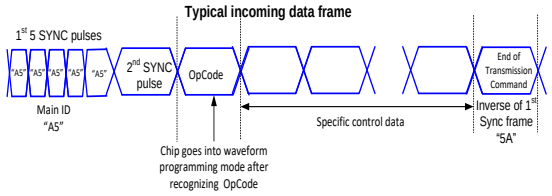


Fig. 4 General structure of the incoming data frame sets that would be received

Our design supports different modes of operations which can be grouped in to housekeeping modes, debug modes and stimulation modes. The housekeeping groups consists of Idle (the default mode), reset and JTAG programming modes. The debug group consists of various commands that allows the external circuits to read out internal states of the design such as the received command, the current mode, the clock frequency and the analog voltages of the front end. Finally, the stimulation group consists of Stimulator parameter, stimulator sequence and stimulator Trigger modes. This paper only focuses on describing the stimulation modes.

To reduce the complexity of the state machines, each mode of operation is implemented as a separate module. The UART decoder, upon successfully decode the OpCode will force the chip to enter the corresponding mode by changing the MODE register and issue a MODE_CHANGE pulse.

III. PROGRAMMABLE STIMULATION CONTROL

The current stimulator chip has multiple channels, each of which is capable of delivering bi-phasic current pulses with programmable pulse width and pulse height (i.e. stimlating duration and current magnitude). Furthremore, each channel must be controlled independently to provide the maximum user flexibility. Finally, the chip is able to store a several sets of stimulating pattens so that the overal stimulating sequence programming can be performed efficiently.

In order to support the above requirements, a compact stimulation sequence encoding scheme was proposed. First, the long term stimulation sequence was broken down in to atomic waveforms, each of which can be presented using 6 bytes (I1, T1, D1, I2, T2, D2), as shown in Fig. 5. Second, an on-chip memory was used to store all desired atomic wavforms. The size of the memory is dependent on the number of long-term storage requirement for some specific applications. Note that the memory content is writelessly programmable thus not all waveforms must be stored at the same time. In this implementation, 40 x 6 = 240 bytes of memory was used for the waveform storage. The atomic waveforms then can be called and combined to create the corresponding sequences for each stimulatio channels. Once all 40 atomic waveforms are programmed to the chip, they can be referred to by their own waveform ID. The waveform ID can then be used to retrieve the actual waveform parameters (i.e. I1, T1, D1, I2, T2, D2) from the waveform memory. Further more, each channel's stimulation sequence can be chosen independently.A specific stimulation sequence requires two parameters: (1) its atomic waveform ID and (2) stimulation duration. Before the actual stimulation, waveform IDs and stimulatio duratios of each channels must be sent to the chip via its wireless link.

It is also worth mentioning that not all channels must be activated. It is also possible to selectively activate some particular channels while the others can be hold inactive, depending on the required stimulus to the muscles. Fig. 6 illustrates the flow chart of a typical stimulation session. Once the chip is power up and enter stable operation mode, users can start programming the atomic sequences using is wireless link. Next, it can enter the sequence programming mode where the actual sequences are constructed using paricular atomic waveform IDs and corresponding duration. Finally, actuall stimluation can be triggered using the stimulation trigger command in which particular sequences are selected and assigned to specific channels. Stimulation ends when all stimulation sequences are completed.

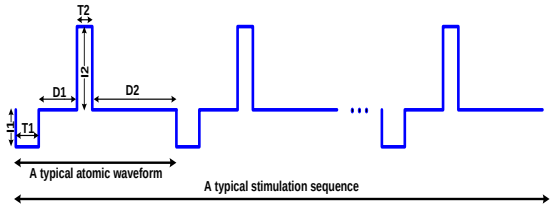


Fig. 5A typical bi-phasic stimulation sequence and its atomic waveform

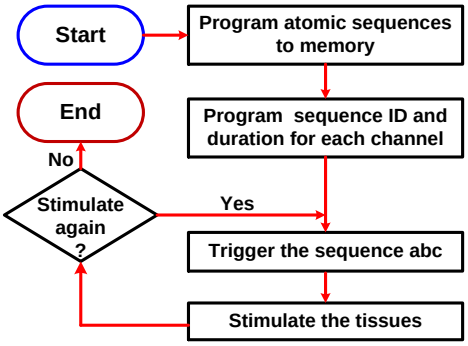


Fig. 6The proposed design's flowchart during stimulation

To faciliate the above testing flow, three different stimulation OpCodes are supported, as described below:

1. Atomic waveforms program mode:

The on-chip registers storing atomic waveforms parameters would be programmed in this mode. The chip enters this mode after receiving the UART command (Fig. 7, and after sending the "ACKNOWLEDGE Good" reply) as shown below. When all the atomic waveforms data has been received and with receipt of the End of transmission frame, the design would exit this mode, enters the Idle mode and wait for next command.

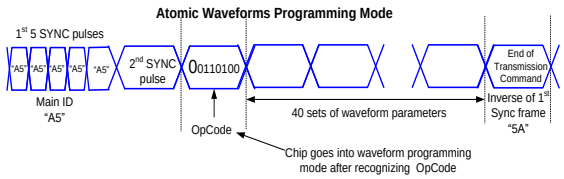


Fig. 7Atomic waveform programming mode command frames

Table I: Data sequence to be programmed to the on-chip registers

Set 1	$T_{1,1}$	$D_{1,1}$	$T_{1,2}$	$D_{1,2}$	$I_{1,1}$	$I_{1,2}$
Set 2	$T_{2,1}$	$D_{2,1}$	$T_{2,2}$	$D_{2,2}$	$I_{2,1}$	$I_{2,2}$
…						
Set 40	$T_{40,1}$	$D_{40,1}$	$T_{40,2}$	$D_{40,2}$	$I_{40,1}$	$I_{40,2}$

2. Stimulation sequences program mode:

Similar to the previous mode, the on-chip registers are used to storethe sequence parameters. The chip enters this mode after receiving the UART command (Fig. 8, and after sending the "ACKNOWLEDGE Good" reply) as shown below. When all the atomic waveforms data has been received and with receipt of the End of transmission frame, the design would exit this mode, enters the Idle mode and wait for next command

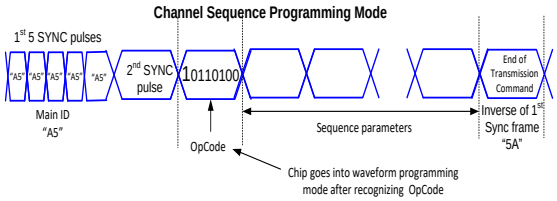


Fig. 8 Stimulator sequence programming command frame

3.Stimulation trigger mode:

The desired stimulation sequence will be triggered in this mode. The chip enters this mode after receiving the UART command (Fig. 9) and after sending the "ACKNOWLEDGE Good" reply) as shown below. Once acknowledged, the stimulation sequence will be executed. If either the channel parameters or sequence parameter registers are all set to "0", the stimulator for that channel would not trigger. When executing the stimulation sequence, any incoming command would be ignored.

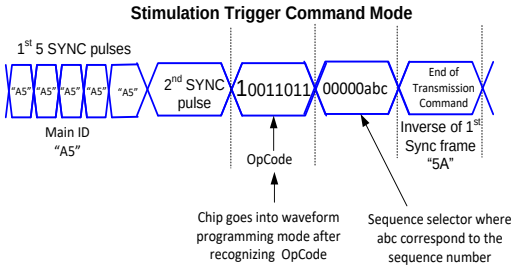


Fig. 9 Stimulator sequence programming command frame

IV. TEST CHIP IMPLEMENTATION

The proposed controller has been implemented using a standard 0.18 um/1.8V CMOS process. Withinthe design, there are two clock domains: (1) Slow clock CLK_S for the UART decoder and (2) fast clock CLK_F for the rest of the circuit.

While CLK_S is in the rage of a few KHz, CLK_F is 3.2 MHz. Therefore, care must be taken of for signals that passed across these two clock domain.

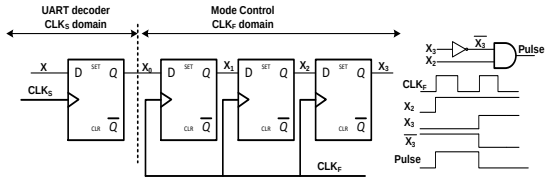


Fig. 10 Resynchronization circuit between two different clock domains.

Fortunately, the only signals that cross this border is the MODE[3:0] and MODE_CHANGE. Once the UART decoder successfully decoded the input command (Fig. 7), it issues a MODE_CHANGE signal and at the same time change the MODE to its new value. Both MODE and MODE_CHANGE are the outputs of the UART decoder and sent to the rest of the circuit. To avoid timing issues and wrong state transition, a re-synchronization circuit (Fig. 10) was used. MODE_CHANGE signal was applied to this circuit to capture the rising edge of the MODE_CHANGE and transforms it to a single clock-cycle pulse in the fast clock domain CLK_F. This signal signify that the chip should enter a new mode.

As also shown in Fig. 11, at the falling edge of single clock-cycle MODE_CHANGE signal (in the fast clock domain), the MODE signal is stable and can be safely registered by CLK_F. This approach allows an elegant and effective handshaking between two domains. After being registered, the MODE signal in the fast clock domain can be used to activate the corresponding blocks within our design. MODE_CHANGE can also be used as a local reset signal, if necessary.

Table II shows the synthesis results in 0.18 um CMOS process. The design's layout is also shown in Fig. 10, occupying XXX um2. Post-layout simulation (Fig. 11) with a comprehensive test bench also confirm that it works properly and produce the exact same output as pre-layout RTL simulation.

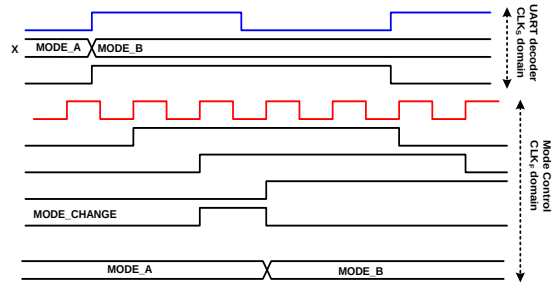


Fig. 11 Timing diagram of the MODE and MODE_CHANGE signal cross the clock domains

Table II: Synthesis results of the design in 0.18um CMOS process

Operating frequency	100 MHz
Set-up violation	0
Hold Violation	0
Area	
Combination cells	2354
Sequential cells	706
Total area	858106

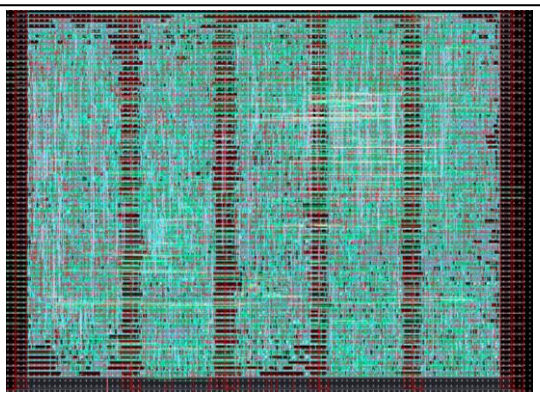


Fig. 10 Final layout of our proposed design .

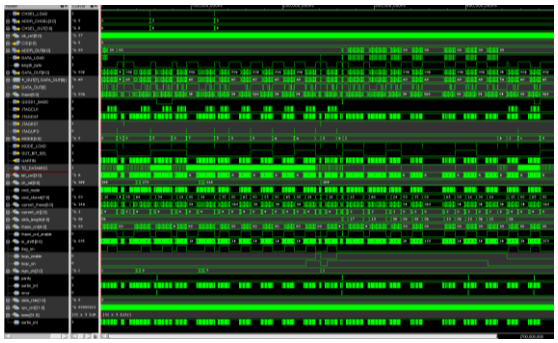


Fig. 10 Resynchronization circuit between two different clock domains.

CONCLUSION

A flexible, user-friendly digital control unit for wireless multi-channel peripheral nerve stimulation application has been implemented in 0.18 um CMOS process. It offers robust operation with various operating modes such as housekeeping, debug and stimulation. Multiple waveforms and sequence combinations can also be programmed and stored on-chip for efficient testing and verification. It is therefore suitable for not only lab-based but also practical prototype developemnt.

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