REPLICA BIASED VOLTAGE CONTROLLED OSCILLATOR FOR SWITCHING REGULATORS

[1]NEELAKANTAN NARASIMMAN, [2]RAVINDER PAL SINGH

[1,2]Integrated Circuit Design Laboratory, Institute of Microelectronics, Singapore
E-mail: 1neeln@ime.a-star.edu.sg, 2ravinderps@ime.a-star.edu.sg

Abstract - In this paper we preset a multi-phase Voltage Controlled Oscillator (VCO) that uses a replica biasing circuit to ensure that the output swing of the VCO is uniformly distributed across a common mode voltage. Since the VCO output swing is regulated across the common mode voltage, the output phases are uniformly distributed. The output phases of the VCO can be used for generating multi-phase switching outputs in voltage regulators. The frequency of oscillation can be controlled using the current source. Proposed scheme was implemented using 0.18□m CMOS technology. It can be seen from the simulation results that the proposed scheme has a wide tuning range of 1MHz-90MHz and can produce 4 uniform phases.

Index Terms - High frequency switching regulators, muli-phase output, replica biasing, VCOs.

I. INTRODUCTION

Most of the portable handheld devices require a power management unit (PMU). These PMUs are essentially a DC-DC converter or an LDO. For better conversion efficiency, a DC-DC converter is preferred (Fig. 1) [1]. It comprises of a high-side switch and a low-side switch which works under the control of a PWM controller.

The size of the output filter in a DC-DC converter depends on the PWM frequency. For reducing the foot-print and PCB real-estate, a high frequency converter is used. Typically, the frequency is set by using an on-chip voltage controlled oscillator (VCO). These VCOs can be realized using delay-cells arranged in a closed-loop.

The output from each delay cell will have a different phase of operation. These multiple phase outputs of the VCO can be a good candidate for a multi-phase DC-DC converter [2]. However, the fine-tuning the operating frequency of such VCO will be a challenging task. For incorporating the fine-tuning in the output frequency, current-starved delay cells are preferred.

Authors in [3, 4] have proposed multi-phase current starved oscillator. However, the linearity and phase parity of the VCO is quite limited. In order to improve the linearity and better phase parity we propose a replica biasing scheme for the VCO.

II. PROPOSED REPLICA BIASED SCHEME FOR VCO

Error! Reference source not found. illustrates a 4-stage VCO biased using a replica biased scheme. Replica biasing circuit is comprised of an op-amp, diode connected PMOS and NMOS device and a 4-stage VCO. Internals of the 4-stage VCO is given in Fig. 3 and are comprised of simple CMOS differential inverter delay cells. The diode connected PMOS and NMOS device in Fig. 2 are of the same size as in VCO delay cell in Fig. 3 and are added to emulate the VCO oscillation transient point where both PMOS and NMOS would be conducting.

A common mode voltage VCM = VDD/2 is internally generated using two PMOS devices. Operational amplifier ensures that the voltage at the midpoint of the NMOS and PMOS diode connected transistors, i.e. VMID = VCM. A compensation capacitor is added as shown in the Fig. 2 to improve the stability. The bias current for the VCO can be tuned by an external current source feeding a diode connected NMOS device. The current thus input, is mirrored to the VCO bias and the frequency of its oscillation can be controlled.

The high gain op-amp in replica bias circuit not only ensures that the midpoint of switching is same as VCM but also improves the linearity of the VCO by ensuring that the input current is fully pumped in. VCO in Fig. 3 also has an enable pin to start/stop the oscillations. Under balanced load conditions, 4-delay stages of the VCO in Fig. 3 naturally produces 4 output phases that are spaced 900 apart from each other. The output phases of the VCO can generate 4 phases of the Pulse Width Modulated signal which could be used for buck operation in multi-phase DC-DC converters.

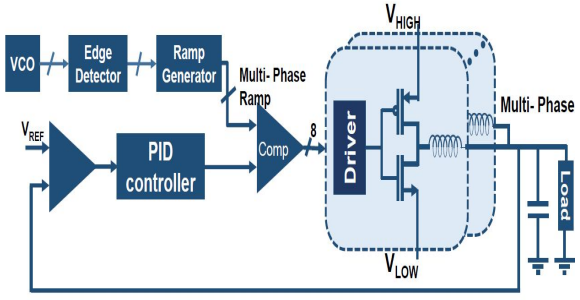


Fig. 1 Typical block diagram representation for a DC-DC Converter

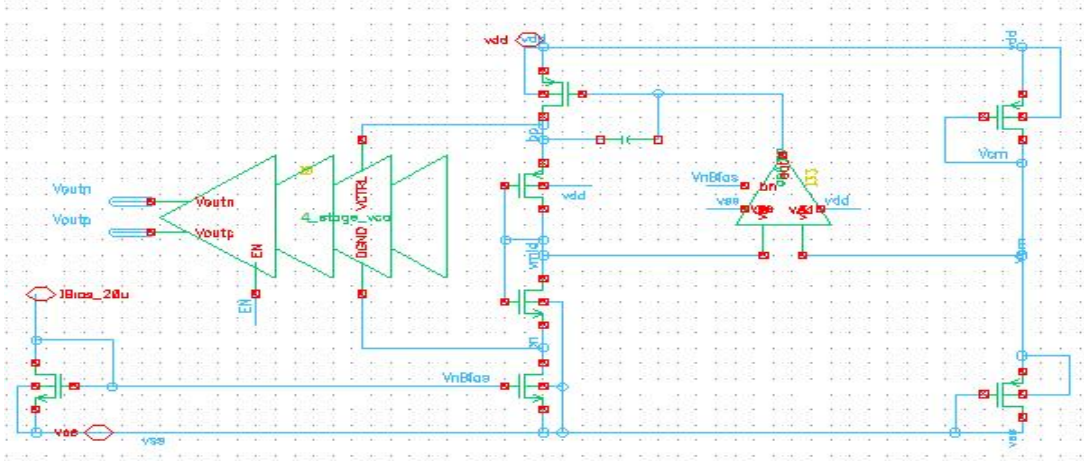


Fig. 3. 4 Stage current starved VCO with Replica Bias

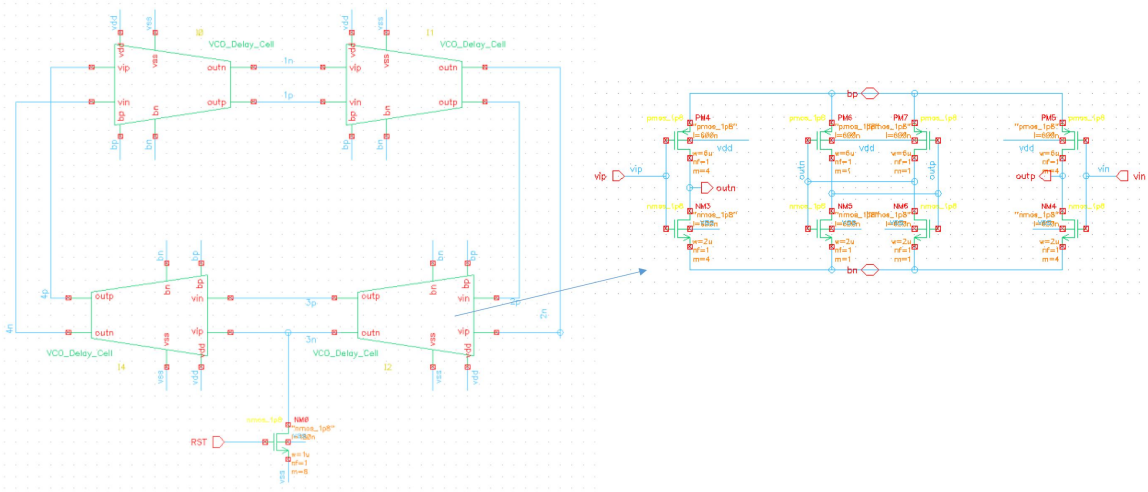


Fig. 2 4 Stage VCO and the delay cell using differential CMOS inverters.

III. SIMULATION RESULTS

The circuit schematic for the proposed sensing scheme was implemented in 0.18um CMOS technology. Layout was drawn using cadence virtuoso and post layout models were extracted to estimate the effect of parasitic on the circuit. Various simulations were performed on the extracted model using Cadence ADE SPECTRE simulations. Fig. 4 illustrates the simulated results for running range of the VCO. It can be seen that the VCO frequency changes linearly for an input current range. The VCO current can therefore be tuned from 0-50uA to obtain a tuning frequency range of 100 kHz to 90MHz. Fig. 4 shows the transient response of the oscillator starting from a power on. It takes around 600ns for the output of the oscillator to stabilize. Fig.4 also illustrates a ramp output which is in sync with the VCO oscillations. The post-layout extracted model was simulated under different process-temperature conditions. Table-1 lists the summary of simulation results for various corner and temperature conditions.. It can be noticed that the proposed oscillator is quite stable across different process corner conditions. The oscillator consumes less than 60uA from a 1.8V power supply.

CONCLUSION

This paper proposes a voltage controlled oscillator with replica biasing scheme. Post-layout simulation results demonstrate good amount of linearity and robustness for the oscillator. The oscillator has a tuning range of approximately 90MHz. The multiple phase output from the oscillator can be used in multi-phase DC-DC converters.

ACKNOWLEDGEMENT

This work was supported by EDB through Office for Space Technology and Industry (OSTIn) – Space Industry Alignment Grant (SIAG) #S15-1323.

REFERENCES

[1] "A RISC-V Vector Processor With Simultaneous-Switching Switched-Capacitor DC–DC Converters in 28 nm FDSOI," B. Zimmer, et.al. , IEEE Journal of Solid-State Circuits, March 2016

[2] Ravinder Pal Singh, Ashwin M. Khambadkone, "Giant Magneto Resistive (GMR) effect based Current Sensing Technique for Low Voltage/High Current Voltage Regulator Modules", IEEE Transactions on Power Electronics, Vol 23, No. 2, March 2008, pp 915-925.

[3] M. Kumngern, J. Chanwutitum and K. Dejhan, "Fully integrated current-mode quadrature sinusoidal oscillator circuit," Proceedings of the 2011 International Conference on Electrical Engineering and Informatics, Bandung, 2011, pp. 1-4. doi: 10.1109/ICEEI.2011.6021802

[4] V. G. Nasre and G. M. Asutkar, "Design of current starved voltage control oscillator with band gap reference in 0.18µm CMOS process," 2017 International Conference on Recent Innovations in Signal processing and Embedded Systems (RISE), Bhopal, 2017, pp. 375-380. doi: 10.1109/RISE.2017.8378185

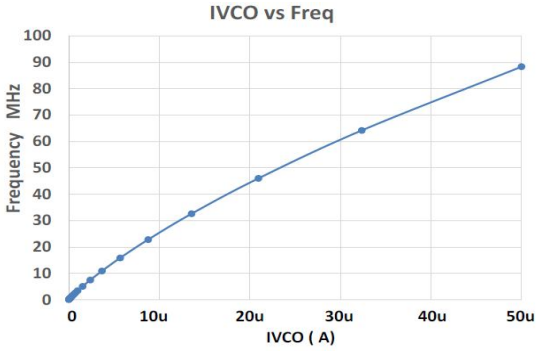


Fig. 4 IVCO vs. Frequency Tuning curve

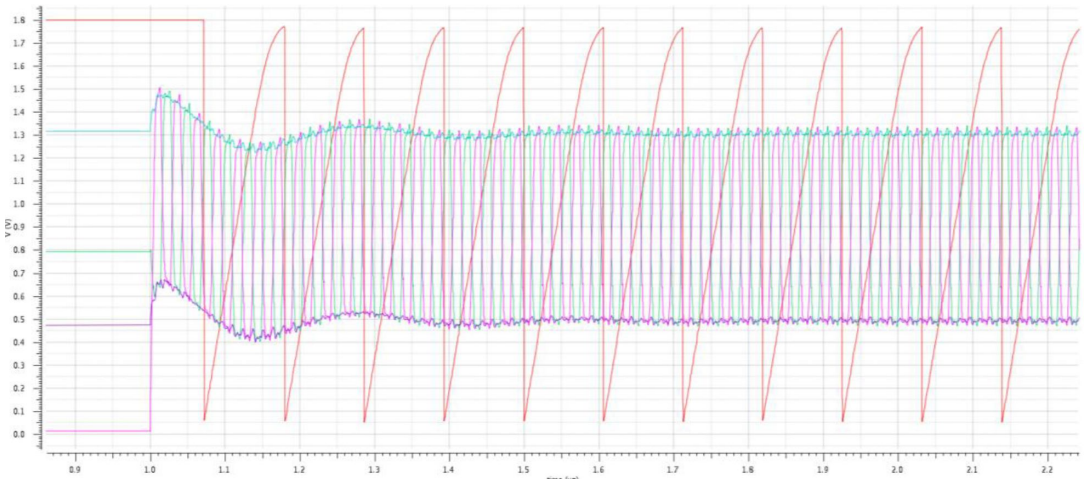


Fig. 5 Simulation results for VCO and ramp output

Table 1 Post Layout Simulation Results For The Vco Across Different Process Temperature Corners

Corner	ff	ff	ff	fs	fs	fs	sf	sf	sf	ss	ss	ss	typ	typ	typ
Temp	-40	30	120	-40	30	120	-40	30	120	-40	30	120	-40	30	120
freq	37.9	37.8	37.7	29.8	31.5	32.6	34.4	34.2	34.1	31.0	31.6	31.7	34.3	34.5	34.5
Ramp Freq	9.5	9.4	9.4	7.4	7.9	8.1	8.6	8.6	8.5	7.8	7.9	7.9	8.6	8.6	8.6

★★★