A 100 MHZ ABOVE 80% EFFICIENCY MULTI-PHASE SWITCHING REGULATOR

[1]CHEMMANDA JOHN LEO, [2]RAVINDER PAL SINGH

2,Fusionopolis Way, #08-02, Innovis, Singapore 138634
E-mail: [1]leocj@ime.a-star.edu.sg, [2]ravinderps@ime.a-star.edu.sg

Abstract - Performance per Watt has become increasingly important metric for microprocessors used in today's mobile devices. Dynamic voltage frequency scaling (DVFS) is widely used approach to improve on the performance/Watt. In this paper, integrated voltage regulator (IVR) type multiphase buck converter switching at 100 MHz providing a maximum load current of 2.0 A is presented, useful in DVFS applications. To realize such high switching frequency converter, all the components including the low-pass filter passives namely inductor and capacitor where made on-chip. In-house magnetic core based inductor for higher inductive density and MOSFET based capacitor are used to realize ASIC with no components on board. Thus, eliminating bottlenecks arising from bond-wire parasitic restricting the response time to few 10s of µs range. The converter output voltage settles within 5-7 clock cycles roughly around 50-70 ns timescale for a step load current change of ΔI_L = 1.0 A. The converter output ripple is also curtailed to few 10s of mV mainly through ripple cancellation using multiphase, plus lower inductor current ripple on account of operating at high switching frequency.

Keywords - Multiphase Buck Converter, Switching Mode Power Supply, Integrated Voltage Regulator, Dynamic Voltage Frequency Scaling, Voltage-mode Controller.

I. INTRODUCTION

Increasingly complex and high performance microprocessors and systems-on-chip (SOC) demands an equally fast and high current throughput power delivery system. Neither the conventional off-chip dc-dc converter nor the bulky off-chip component based dc-dc converter operating with response time in few tens of micro seconds (µs) range can able to meet the dynamic response in sub-µs range of the processors used in modern mobile gadgets. Another important parameter that equally deserve attention for these mobile processors is the performance per Watt as these devices is constrained by limited amount of energy that the battery can store. In order to improve on the performance per Watt (PPW), dynamic voltage and frequency scaling (DVFS) technique is widely used which dynamically adjust the supply voltage and operating frequency depending on the computational intensity of the processor [1].

However, the time scale over which supply voltage and frequency is varied directly influence the efficacy of the DVFS technique. In general, a faster voltage transition in sub-µs range results in a more efficient DVFS implementation [2,3]. Hence, from the perspective of both speed and PPW, it is quite natural to move towards a fully integrated on-chip dc-dc converter. On-chip step-down converter can be implemented in many ways such as low-dropout linear regulator, switched capacitor based converter and buck converter. Each has pros and cons depending on the applications, cost and ease of design, however buck converter with on-chip passives are pursued quite intensely in recent times for its high efficiency over wide range of V_{out} though realizing high quality on-chip magnetic core inductor is still a bottleneck. In order to realize on-chip passives, the size of the passives needs to be reduced which results in switching frequency being pushed to higher values which has the additional benefit of realizing fast transient response converter suitable for DVFS application [4,5]. Realizing on-chip inductor with reasonable inductance values within a small area necessitates the usage of magnetic-core power inductors which are capable of delivering large current density in few A/mm^2 range [6]. On the other hand, integrating on-chip decoupling capacitor though implemented using MOS-capacitance still result in only a couple of nanoFarad capacitance, thus resulting in large converter output voltage ripple. Multiphase buck converter is generally implemented to minimize the output voltage ripple through ripple cancellation from different phases being phased out in time since all the phases share a common output node. Multiphase implementation also help improves the efficiency of the buck converter by dividing the current through each phase ideally in equal proportion thus reducing the dc power-loss in square terms proportionally.
Accordingly in this work, a tunable multiphase buck converter is designed with a switching frequency of 100 MHz regulating the output at 1.0 V from a 1.8 V input supply.

The converter operates with maximum phases of eight during high load condition and minimum number of phases of two during low load condition. Section 2 describes the topology and operation of the single-phase buck converter and later explains the advantages of using multiphase buck converter. In section 3, the simulation results of the compensator block as well as the top level buck converter under different load conditions and varying the phases in tandem is presented and explained.

II. SYSTEM DESIGN

2.1. Single Phase Buck Converter

A conventional single-phase buck converter is shown in Fig.1. which is comprised of four main blocks namely: 1. Power-Stage, 2. Compensator, 3. Pulse Width Modulation (PWM) block and 4. Driver block. Power-stage block includes power switches in half-bridge configuration and inductor (L) – capacitor (C) based low-pass filter whose resonance frequency is kept smaller than the switching frequency to avoid clocking disturbance entering into the system. Since the LC filter is a second-order system, it is inevitably unstable. So, when placed in a closed-loop, a compensator block is commonly used to make the system stable. In general, a type-III compensator is used to provide a large dc gain for a good steady-state response as well as a stable operation by boosting the phase-margin up to the frequency band of interest.

Since the input voltage of the converter is 1.8V, a conventional power switch half-bridge configuration cannot be used with thin gate-oxide MOS transistor device as the voltage drop across the device exceeds the maximum voltage difference V_{max} permitted by the CMOS technology, resulting in reliability issues. On the other hand, using thick gate-oxide MOS devices results in higher conduction losses on account of higher intrinsic device resistance. Hence, a cascode bridge configuration using thin gate-oxide devices is used which overcomes the problem by maintaining the voltage across the devices within the tolerance limit. The clock with required switching frequency is either generated on-chip or provided externally and used for generating ramp, which is then compared against the voltage output from the compensator for generating clock with appropriate duty-cycle as the PWM output. Power switches in half-bridge configuration can be realized with either switches being PMOS switches or NMOS switches or can be PMOS-NMOS switches. Depending on the type of switches used non-overlapping clock (NOC) is generated from the PWM output and buffered using cascaded driver stages to drive the bulky power switches. Depending on the maximum load current ($I_{L,max}$) the power-stage has to support, the size of the power switches is decided. A large switch will have lower intrinsic resistance and hence a lower conduction loss. On the other hand, a large switch will have larger parasitic gate capacitance and hence a larger switching loss. Thus, the size of the power switches needs to be optimized by finding the minima of the sum of conduction and switching losses to enhance efficiency. The overall efficiency of the buck converter is calculated using the equation:

$$\eta = \frac{P_{load}}{P_{in}} \qquad \ldots\ldots (1)$$

where, P_{load} is the power delivered to the load and P_{in} is the input power which includes the output power as well as all the losses namely conduction and switching losses incurred in the switch, inductor, capacitor, driver and the controller.

2.2. Multiphase Buck Converter

Integrated Voltage Regulator (IVR) is paramount to realizing high switching speed for its implementation in DVFS applications. Realizing the passives on-chip is made possible by increasing the switching frequency to higher value allowing a corresponding increase in resonance frequency thus enabling a reduction in passive values and hence its size accordingly. In order to realize inductor of reasonable value within a small area, thin-film inductor with magnetic-core of high magnetic permeability is used. However, the downside is that the total equivalent resistance of the magnetic-core inductor is almost an order higher than air-core based inductor resulting in large conduction power loss degrading efficiency. Multiphase buck converter help minimize the loss by splitting the current among the different phases thus reducing the I^2R loss in square terms.

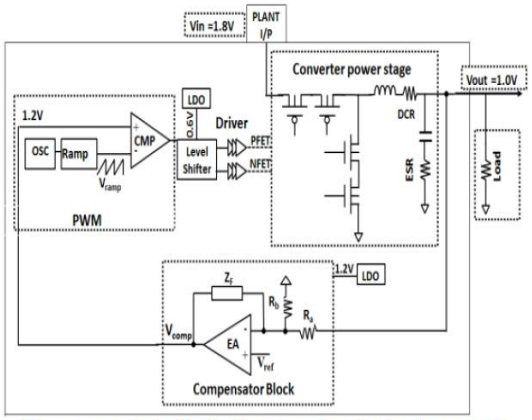


Fig.1. Schematic block diagram of a single-phase Buck Converter

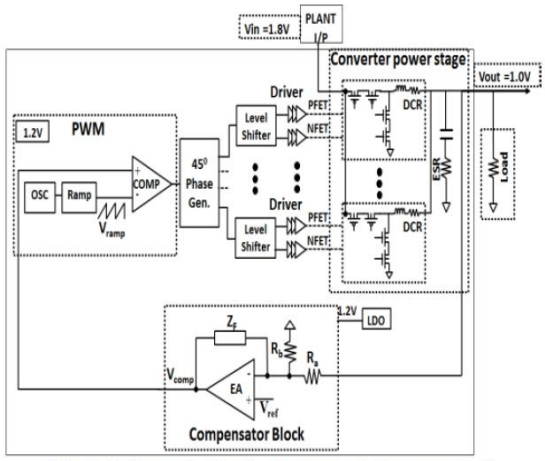


Fig.2. Schematic block diagram of the proposed multiphase Buck Converter

Another drawback of using inductor with magnetic core is the magnetic material becomes saturated beyond a certain magnetic field strength forcing an upper bound to the current that a phase of the buck

converter can support. To extend the operation region limited by current saturation, coupled inductor is used to avoid dc saturation by letting the two signals to flow in opposite direction thus neutralizing the dipoles from being aligned in one direction.

Also, complementary signals that are out-of-phase by 180^0 is used in the coupled inductor such that ac magnetic field adds up increasing the mutual inductance resulting in decreased inductor current ripple. Accordingly, an eight phase buck converter is proposed as shown in Fig.2 using four coupled inductors with the different phases switched at the same switching frequency but in a time interleaved manner.

The inductor has been modelled using the S-model parameters obtained from simulating the inductor using the field solver Agilent's Advanced Design System (ADS). Later, the accuracy of the simulation results is verified by comparing with the measurement results of the fabricated inductor.

III. RESULTS AND DISCUSSION

Multiphase buck converter proposed in this work is designed in 55nm technology node. The total chip area measure 3.0 x 3.0 sq.mm. Since the process technology used is a shrink version of 65nm, a 10% linear shrink is expected over the total area and hence the fabricated chip will be of the dimension 2.7 x 2.7 sq.mm. The on-chip output filter MOSFET capacitor occupies major portion of the chip area. The inductor is fabricated on a carrier silicon interposer chip and the ASIC chip will be flip chipped on the carrier chip. All the results presented in this paper were simulated using the Cadence Spectre circuit simulator analysis tool.

3.1. Compensator Block

The resonance frequency of the tank circuit with the inductor (L = 10 nH) and the capacitor (C = 10 nF) with a single phase is around 35 MHz and with eight phases is around 100 MHz.

Since the closed-loop bandwidth (BW) of the system is designed to be around 10 MHz, the second order complex poles of the LC filter lie outside the loop BW and does not degrade the phase margin significantly around the corner frequency (f_c). Hence, a type-II compensator suffices and used in this work to keep the loop stable. Bode plot of the type-II compensator as well as the plot of tank + compensator blocks are shown in Fig.3. As expected, the LC complex poles effect is seen around the f_c however the phase-margin (PM) is maintained sufficiently large around 80^0 across the corners even with a single inductor which is the worst-case scenario since at least two phases will be turned ON at any given time to keep the inductor current ripple lower.

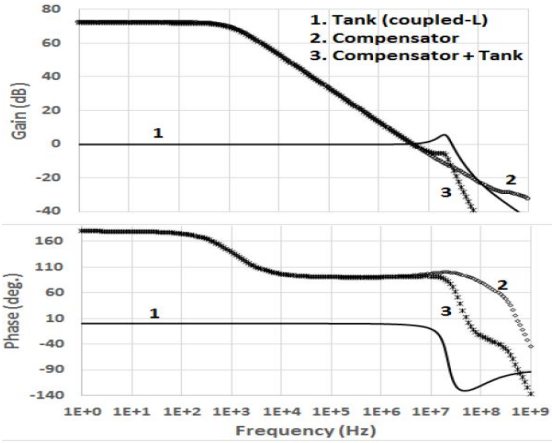


Fig.3. Bode plot showing the gain and phase of the Tank; Compensator and Tank + Compensator

3.2. Optimized Transient response

This section specifies the load transient response of the closed-loop multiphase system where the number of phases is adjusted according to the load it support. Transient analysis on the overall closed-loop system is performed by varying the load in discrete steps of 250 mA, 500 mA, 1.0 A and 2.0 A with the number of phases varied in accordance as 2, 4 and 8 respectively. The transient simulation results is shown in Fig.4. with the top waveform showing the converter's output voltage variation as a function of time when the load current is changed in time steps of 10 ns as seen in the bottom waveform. The maximum excursion in the output voltage are seen when a load current step of 1.0 A to 2.0 A and later from 2.0 A to 1.0 A in 10 ns is applied. When load current step up, an undershoot of ~150 mV and when load current step down, an overshoot of 220 mV are seen with a settling time of ~20 ns and ~30 ns respectively.

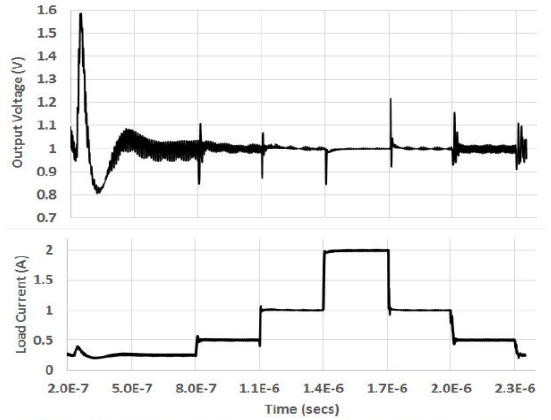


Fig.4. Transient analysis showing converter's output voltage with change in load current

On account of large closed-loop BW of the system enabled by high switching frequency, the settling time achieved is in few 10's of ns and fulfil the requirement for DVFS application. The output voltage ripple is seen larger ~86 mV for low load condition (I_L = 250 mA) compared to the ~8 mV output ripple seen during the high load condition ($I_L \geq$

1.0 A) almost an order of magnitude smaller. This is because during the low load condition not all the phases are turned on resulting in lower ripple cancellation. The inductor current ripple for the multiphase buck converter is given by:

$$\Delta I_L = \frac{V_o(1-D)}{L*f_s} * \frac{N(D-\frac{m}{N})(\frac{m+1}{N}-D)}{D(1-D)} \quad \ldots\ldots (2)$$

where, m = floor (D, N) and m is an integer not exceeding D*N, N is the number of phases, D is the duty cycle, f_s is the switching frequency, L the inductance and V_0 is the converter output voltage. The first term signifies the inductor current ripple for a single phase and the second term signifies the ripple current cancellation factor. So, from eqn. (2) it can be deduced that the inductor current ripple becomes smaller with increasing number of phases as a result of the second term getting smaller with increasing number of phases and is more pronounced for higher duty cycle. The efficiency of the multiphase buck converter for different load conditions where the number of phases were adjusted accordingly while regulating the output at 1.0 V is tabulated in Table 1. The detail of the total losses incurred by various devices of the buck converter for a load current of 1.0 A where all eight phases are on is shown in a pie-chart in Fig.5.

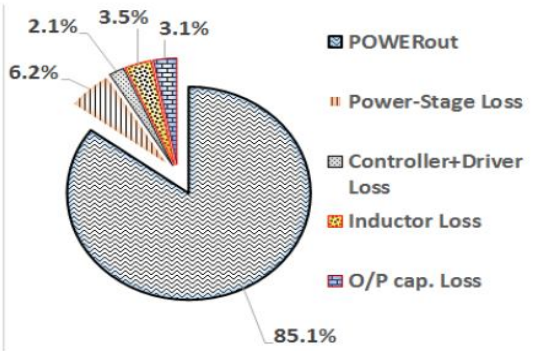


Fig.5. Pie chart showing the total efficiency and losses incurred by converter's various devices

The power-loss incurred in the power-FET switches dominate among the different losses, almost double when compared to inductor loss for a load of 1.0 A. This power switches loss is process technology dependent and has little scope to improve unless otherwise the PDK (Process Design Kit) is changed. The inductor loss has ac and dc components given by:

$$P_L = P_{dc} + P_{ac} \quad \ldots\ldots\ldots (3)$$

$$P_L = \{(I_{dc}^2 + \frac{I_{ripple}^2}{12}) * R_{L_DCR}\} + P_{ac} \quad \ldots\ldots (4)$$

where, R_{L_DCR} is the dc resistance of the inductor dependent on the inductor geometry and the ac power loss depends on many parameters such as the effective core volume of the inductor, magnetic core loss parameters that are material dependent, switching frequency and peak flux density.

The inductor loss increases steeply with the load and is almost comparable to power switch loss in the high load condition as can be seen in the Table.1 mainly on account of inductor ac-loss increasing significantly on top of the quadratic increase of the inductor dc-loss component. For a load of 2.0 A, the inductor loss is 6.5% which is comparable to the power switch loss of 7.6%. Hence, for high power applications the inductor loss is the major contributor for efficiency degradation and accounts for more than 60% of the total power loss [7].

Table 1: Table showing input and output power, efficiency and the breakdown of the various losses for different load conditions and phases

P_{in} (W)	P_{out} (W)	Load (Ω)	No. of Phases	LOSSES				Total Losses (mW)	Efficiency (%)
				High SW ($I^2R+IV_{overlap}$) (mW)	Low SW ($I^2R+IV_{overlap}$) (mW)	Compensator + Driver (mW)	Inductor (mW)		
0.30	0.2	0.25	2	12.2	4.7	13.3	4.5	34.7	83.4
0.59	0.5	0.50	4	26.9	9.6	16.5	11.1	64.0	84.5
1.18	1.0	1.00	8	53.5	19.6	24.2	41.6	138.9	85.1
2.38	2.0	2.00	8	130.8	51.2	24.2	155.4	361.6	83.9

3.3. Dynamic Voltage Frequency Scaling (DVFS)

The dynamic voltage scaling ability of the multiphase buck converter is validated by varying the reference voltage (V_{ref}) of the controller block in steps of 120 mV, thus forcing the converter output to vary by 200 mV for each step change as seen in Fig.6. The converter output can be seen to settle to the new voltage value within a settling time of two clock cycles, roughly around 20 ns for a load current change in the same proportion keeping the load resistance unchanged. The ability of the buck converter designed to track the reference voltage in the nanosecond timescale enables it to be a good candidate for the DVFS applications.

CONCLUSIONS

A fully integrated multiphase buck converter switching at 100 MHz with a peak efficiency of ~85% for a load of 1.0 A has been reported. A settling time of around 50 ns is achieved for a step load current change of 1.0 A, realizing a fast transient load response buck converter.

Using an external knob to vary V_{ref}, the buck converter output is varied from 0.6 V to 1.2 V with settling time in nanosecond timescale, validating the function of dynamically scaling the output voltage for DVFS application. With varying load, the number of phases is also varied in-tandem to maintain a somewhat constant efficiency over the entire load range.

ACKNOWLEDGMENTS

This work was supported by A*STAR Science and Engineering Research Council (SERC) Grant #152 78 00039. We would also like to thank Global Foundry, Singapore for their support.

REFERENCES

[1] P. Macken, M. Degrauwe, M.V. Paemel and H. Oguey, "A voltage reduction technique for digital systems", IEEE ISSCC Dig., pp. 238-239, 1990.

[2] W. Kim, D. Brooks and G.Y. Wei, "A fully-integrated 3-level dc-dc converter for nanosecond-scale dvfs", IEEE J. Solid State Circuits, vol.47, pp.206-219, 2012.

[3] W. Kim, M.S. Gupta, G. Wei and D.M. Brooks, "System level analysis of fast, per-core DVFS using on-chip switching regulators", IEEE 14th Int. Symp. High performance computer architecture, 16-20, pp.123-34, 2008.

[4] C. Huang and P.K.T. Mok, "An 84.7% efficiency 100 MHz package bondwire-based fully integrated buck converter with precise DCM operation and enhance light-load efficiency" , IEEE J. Solid State Circuits, vol.48, pp.2595-2607, 2013.

[5] J. Wibben and R. Harjani, "A high-efficiency dc-dc converter using 2 nH integrated inductors", IEEE J. Solid State Circuits, vol.43, pp.844-854, 2008.

[6] N. Sturcken, M. Petracca, S. Warren, P. Mantovani, L.P. Carloni, A.V. Peterchev and K.L. Shepard, "A switched-inductor integrated voltage regulator with nonlinear feedback and network-on-chip load in 45 nm SOI", IEEE J. Solid State Circuits, vol.47, pp.1935-1945, 2012.

[7] N. Sturcken, E.J. O'Sullivan, N. Wang, P. Herget, B.C. Webb, L.T. Romankiw, M. Petracca, R. Davies, R.E. Fontana, G.M. Decad, I.J. Kymissis, A.V. Peterchev, L.P. Carloni, W.J. Gallagher and K.L. Shepard, "A 2.5D integrated voltage regulator using coupled-magnetic-core inductors on Silicon interposer", IEEE J. Solid State Circuits, vol.48, pp.244-254, 2013.

★★★