1.5V TO 1.2V LOW-DROPOUT REGULATOR (LDO) FOR LOW POWER APPLICATIONS

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Abstract - A stable and efficient Low-Dropout Regulator (LDO) is reported in this paper, with 1A output current capability. The LDO converts a 1.5V input to 1.2V output. It uses a two-stage amplifier to achieve large DC gain. An output capacitor is used to provide the high PSRR. Compensation capacitor is added to ensure stability. The IC is fabricated using 130nm CMOS technology node and the measurement results are presented. Line regulation and load regulation of LDO are measured to be 6.4mV/V and 5mV/A respectively.

Keywords - LDO; Efficiency; Power Management; Drop-out; Regulator

I. INTRODUCTION

Regulators and power converters have a huge role to play in modern day electrical systems. While efficient step-down and step-up converters are in demand to obtain the desired voltage required by the end-applications, often the power converter outputs are not regulated. Additionally, owing to the usage of non-linear passive elements such as inductors and capacitors, the ripples at the output are greater than tolerable limits, which may result in consistencies in the applications. Often the output voltage of these converters is filtered using an LDO.

LDOs are linear regulators which employ an error amp with a large gain, a pass transistor switch, a feedback network and an output capacitor to store the charges, as depicted in Figure 1. The challenges in the design include stability, a large dc gain, and low offset from desired output voltage. In addition, the dropout voltage ($V_{DO} = V_{LDO} - V_{DD}$) should be small so as to achieve better efficiency. A larger dropout will result in efficiency drop.

In this paper, we propose an LDO with large dc gain and is stable while delivering output currents upto 1A. At first, we present the proposed LDO architecture, followed by analyses and observation from simulations, which will be followed by the measurement results, and conclusion.

II. CIRCUIT DESCRIPTION & ANALYSES

Figure 2 below is the circuit diagram of the LDO block. The error amplifer is a two-staged amplifier, where for the first stage differential gain amplifier, folded cascode is used to ensure large DC gain. An on-chip compensation capacitor is added to ensure stability, by the introduction of a miller pole [2,3]. A large external output capacitor (33uF) is used to generate a dominant pole for the LDO. It also ensures that the LDO has a large PSRR and is stable. The efficiency is optimized by minimizing the quiescent current of the LDO and also by minimizing the voltage drop or the dropout voltage of the LDO. A reference voltage is generated using an on-chip bandgap voltage reference (V_{REF}). The output voltage is compared with the reference voltage by the error amplifier and produces the control signal for the transistor MN. As our reference voltage is ~1.2V, the feedback ratio=1 (no resistor divider is needed). Thus, under steady state, the two inputs of the error amplifier are equal; thereby maintaining the output voltage regulated at $V_{LDO}=V_{REF}$.

Figure 3 shows the simulation results showing the ac response of the LDO. The phase margin is obtained to be 77°, with an open loop DC-gain of the system is 53dB. The simulated PSRR at 10MHz is obtained as 57dB, as shown in Figure 4. The load regulation of the LDO is simulated by switching the output current from no-load to full-load. The simulated response of load regulation is shown in Figure 5. Ignoring the load transients, the output voltage of the LDO is found to be stable, having load regulation of 1mV/A under steady-state. The summary of various simulation results across process corners is summarized in Table I.

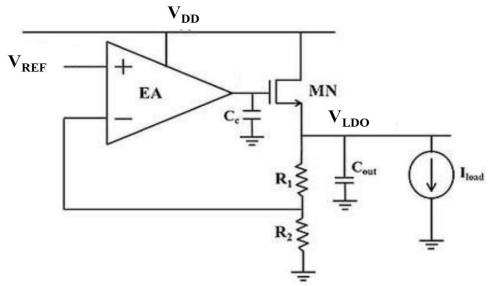


Figure 1. Conventional LDO topology [1]

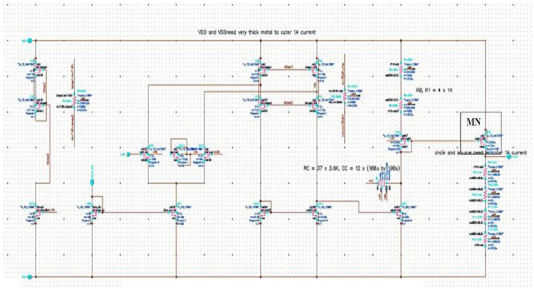


Figure 2. Proposed LDO's architechture

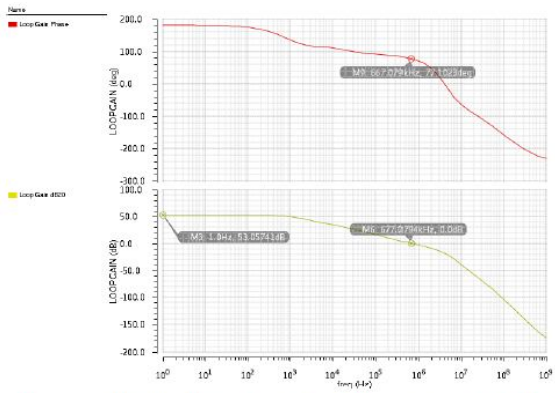


Figure 3. Simulated gain margin and phase margin of LDO

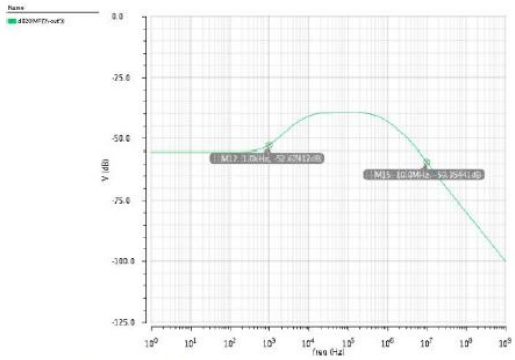


Figure 4. Simulated PSRR response of LDO

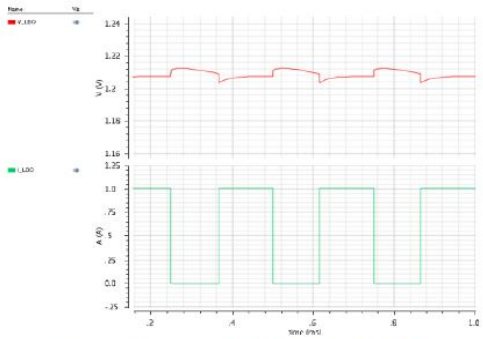


Figure 5. Simulated load transient of LDO

Table I. Summary of simulation results across corners					
		Corners			
		SS	TT	FF	
V_{LDO}		1.191	1.209	1.212	V
PSRR	@1KHz	-42.30	-59.04	-63.00	dB
	@10MHz	-58.46	-57.64	-57.34	
Line Reg.		5.47	1.07	0.87	mV/V
Load Reg.		0.88	0.95	1.19	mV/A

III. MEASUREMENT RESULTS

The circuit has been designed in 130nm CMOS technology. The tests have been performed on the designed PCB containing the ASIC and other necessary components. The proposed LDO is a part of the larger power management unit (PMU) [4], as shown in the chip micrograph of Figure 6. For characterizing the system, the LDO's output voltage is measured by providing a 1.5V at its input pin. The line regulation is measured by varying its supply by 10% around its nominal value and measuring the LDO output. The measured results are shown in Fig. 7. The results measured from three different samples have line regulation of 6~8mV/V as seen from the slope of the curves.

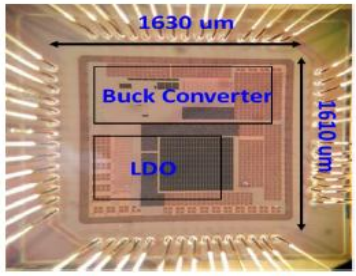


Figure 6. Chip Micrograph of Power Management Unit

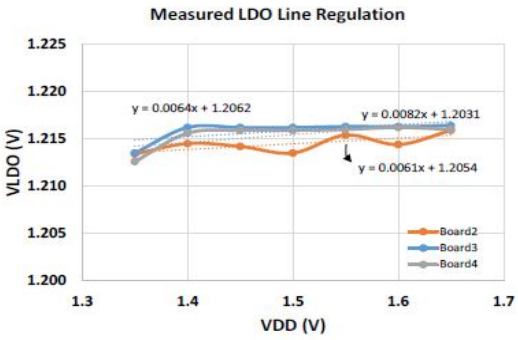


Figure 7. LDO Line Regulation results from 3 samples

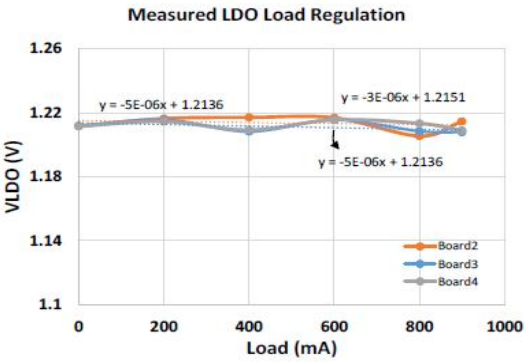


Figure 8. LDO Load Regulation results from 3 samples

While keeping the input supply to the LDO at 1.5V, the measured load regulation results from three different samples are shown in Figure 8. The load regulation is obtained using the slope of the curves. The measured load regulation is found to be around 5mV/A.

CONCLUSION

In this paper, a stable and efficient LDO is reported. It is realized with a two-stage amplifier gain stage, with one-output capacitor and an on-chip compensation capacitor. The output capacitor is

designed large so as to provide a dominant pole and large PSRR. Error amplifier uses a folded-cascode topology for improving the dc gain. Miller compensation capacitor added on-chip, ensures stability. The LDO converts a 1.5V input to a regulated 1.2V output with 1A driving capability. The proposed LDO is implemented in 130nm CMOS technology node and characterized in the lab. The measured line and load regulation is 6mV/V and 5mV/A respectively.

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