# A 10MHZ, 2.5 V TO 1.2 V TWO-STAGE POWER CONVERTER FOR ON-CHIP APPLICATIONS

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**Abstract** - An efficient, high frequency power management unit (PMU) is reported in this paper. The PMU comprises of a front-end buck converter and a second-stage Low Drop-Out Regulator (LDO). The PMU converts 2.5V from battery power supply to a 1.2V output, with 1A load current capability. The IC is fabricated using 130nm CMOS technology node and occupies an active area of 1.6x1.6mm$^{2.}$ The tested chip has an average end-to-end efficiency of 73 % and is suitable for powering on-chip loads.

**Keywords** - Power management; DC-DC Converter; Buck Converter; LDO

## I. INTRODUCTION

AS the demands for products with higher performance are increasing by the day, the economic and technical challenges to reduce transistor sizes and silicon area are also increasing alongside according to the Moore's Law. More recently, a wave of 2.5-D and 3-D IC has emerged, as a result we start advancing beyond the challenges presented by the Moore's law. Through the use of large number of Through-Silicon Vias (TSVs), such 2.5-D and 3-D IC technology results in small form factor and also achieves performance improvements [1, 5]. Nonetheless, all these devices require active power delivery networks which meet the various supply demands. One way to do that is by having individual PMUs on each of these chips. Alternately, a common PMU can be realized on an interposer which can power a group of ICs. However, in this case the output current requirement may be high, upto 1A which poses its own design challenges.

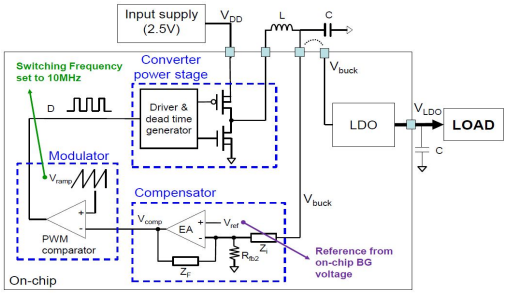


**Figure 1. Proposed PMU Architecture**

In this paper, we propose an efficient PMU suitable for such applications. Detailed design considerations, its operations are presented along with the appropriate measurement results.

## II. PROPOSED PMU & IT'S OPERATION

A system block diagram is showed in Figure 1. It comprises of a front-end buck converter for high-efficiency and a back-end LDO for tight output voltage regulation. Most of the constituent blocks are on-chip. Three off chip components are required for this PMU, namely inductor and capacitor for the buck converter, and an output capacitor for the LDO. In order to have better testability, the output of the buck converter and the input of the LDO are not connected on the chip, rather they are connected at a PCB level.

The size of the output filter inductor and capacitor is inversely proportional to the switching frequency of the buck converter. High switching frequency will help in reducing the size of these components, but may result in increased switching losses. On the other hand, a lower switching frequency can reduce the losses, but will require bigger external components. As a trade-off, the switching frequency for the buck converter is set as 10MHz so as to have relatively small size of output filter inductor and capacitor. In order to reduce the switching losses due to selection of high switching frequency, the gate-drivers are carefully designed. Non-overlapping clock signals are implemented, so as to avoid the simultaneous turning on of both the high side and low side switches. A dead-time is also added before the driver to minimize shoot-through current at the power MOSFETs when both PMOS and NMOS are turned on. Similarly, the conduction loss is reduced by optimally sizing the high side PMOS and low side NMOS power switches. The clock signals to drive these power switches, are duty cycled with the aid of PWM Controller. Duty cycle or duty ratio (D) is defined as the percentage of pulse on-duration ($T_{on}$) to the total period (T) of the waveform. For the given duty cycle, the output voltage ($V_{buck}$) of the buck converter can be expressed by the function of input voltage ($V_{DD}$) and duty cycle (D) as:

$$V_{buck} = D.V_{DD}$$

The buck converter uses an external inductor of 120nH and an external capacitor of 330nF. Frequency compensation is needed to ensure that the system remains stable. Stability of the Buck Converter is ensured by using type-II [2-4] frequency compensator, which is realized on-chip.

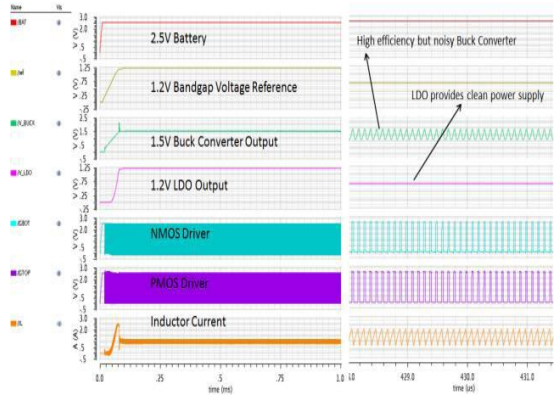


**Figure 2. Start-up transient and steady-state waveforms**

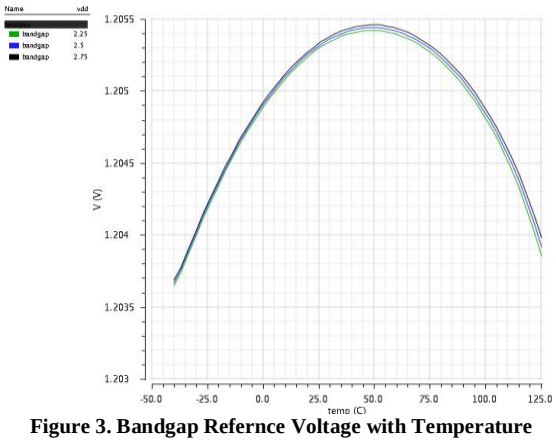


**Figure 3. Bandgap Refernce Voltage with Temperature**

**TABLE I: Summary of simulation results**

| Parameters | Value | | | Unit |
|---|---|---|---|---|
| | SS | Typ | FF | |
| Reference ($V_{REF}$) | 1.192 | 1.21 | 1.213 | V |
| Output $V_{BUCK}$ | 1.487 | 1.511 | 1.516 | V |
| Switching Freq | 8.09 | 9.88 | 11.09 | MHz |
| Buck Efficiency | 75.12 | 82.54 | 86.50 | % |
| Buck Line Reg. | 9.79 | 7.18 | 8.7 | mV/V |
| Buck Load Reg. | 3.18 | 4.79 | 0.02 | mV/A |
| Buck output ripple | 14.09 | 19.63 | 21.06 | mV |
| NOC delay | 1.72 | 0.93 | 0.57 | ns |
| Output $V_{LDO}$ | 1.191 | 1.209 | 1.212 | V |
| Line Reg. | 5.47 | 1.07 | 0.87 | mV/V |
| Load Reg. | 0.88 | 0.95 | 1.19 | mV/A |

Although, the buck converter output can be stable, but it has ripple due to its switching states. The ripple at the final output is minimized by having an LDO as the last stage. Efficiency is maximized by minimizing voltage drop across the LDO.

The LDO consists of a two-staged amplifier, used with folded cascode configuration as the first stage. An on-chip compensation capacitor is added to ensure stability. A large external output capacitor (33uF) is used to generate a dominant pole of the LDO and to achieve high PSRR.

## III. SIMULATION RESULTS & DISCUSSION

Figure 2 shows the simulation results of the full system and the intermediate steady state waveforms. The graphs on the right hand side show the zoomed-in view of the graphs on the left hand side. It can be observed, that a 2.5V battery input to the system, provides 1.5V at the Buck converter's output. The LDO output is 1.2V, as explained previously, to further step-down the voltage from 1.5V and provide a cleaner voltage at the output.

Figure 3 shows the simulation results of the on-chip bandgap reference ($V_{ref}$) generator's performance across temperature range -40°C to 125°C for 3-different supply voltages of 2.25V, 2.5V and 2.75V. The simulation results show <2mV change in reference voltage across these voltage and temperature variations. Slightly higher variations may be seen under different process corners.

Thus, the PMU has been simulated and characterized to validate its performance under varying line and load conditions and analyzed for its stability and functionality under different process corners. The summary of simulation results is presented in the Table I.

## IV. MEASUREMENT RESULTS

The chip was fabricated in 130nm CMOS technology. The chip micrograph of the same is shown in Figure 4, which shows both the buck controller and the LDO.

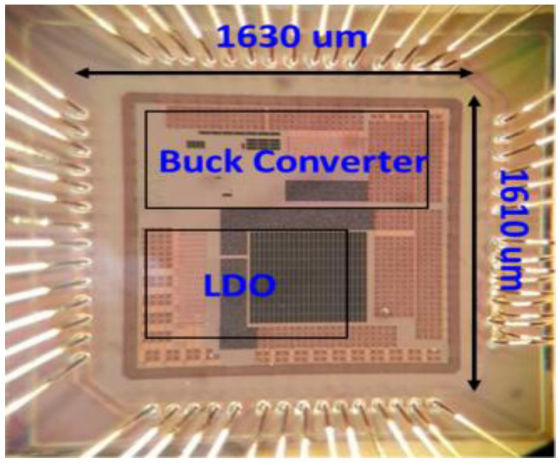


**Figure 4. Chip Micrograph of Power Management Unit**

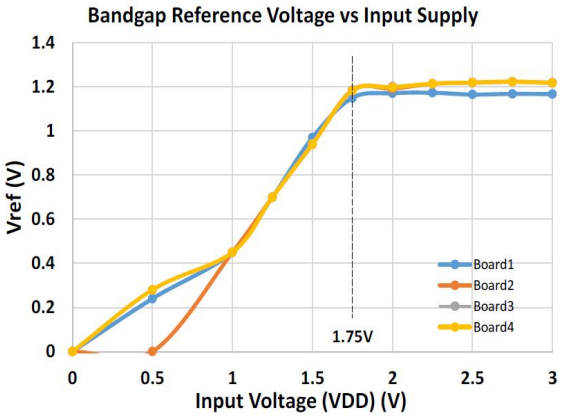


**Figure 5. Bandgap Line regulation Test**

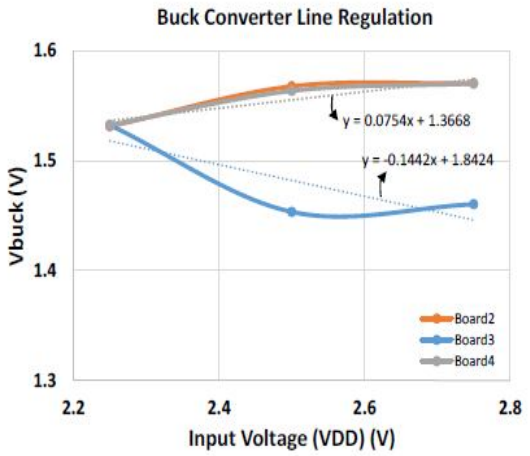


Figure 6. Buck Converter's Line Regulation Test

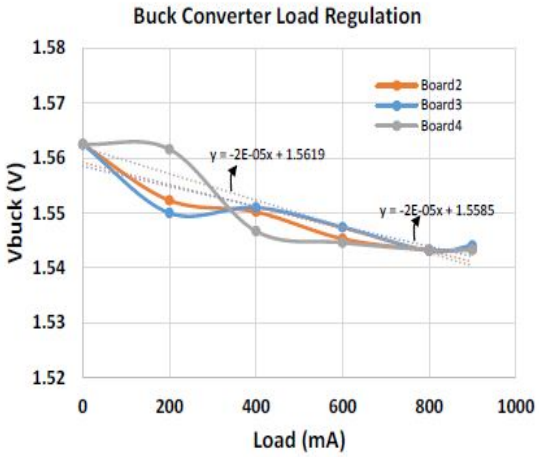


Figure 7. Buck Converter's Load Regulation Test

Line regulation of the bandgap reference block is measured by varying the input supply voltage (VDD) from 0 to 3V and measuring the bandgap reference output. The standalone Bandgap reference is measured on 4 sample boards and the measured results are shown in Figure 5. Although the typical input voltage is 2.5V, the results show it can provide a stable output even at 1.7V input supply. The marginal differences between the behaviors of the 4 boards can be attributed to variations among the chips. Furthermore, around the nominal supply voltage of 2.5V, the line regulation of $V_{ref}$ is measured to be 3mV~8mV/V.

1.0
2.0
3.0
4.0

### 4.1 Buck Converter Line and Load Regulation

Buck converter's output voltage is measured at $V_{BUCK}$ pin. For line regulation analysis, the load at the buck converter's output is kept fixed, and the LDO is isolated from the Buck converter. Line regulation is obtained by varying the input supply voltage (VDD) by 10% around its normal operating point of 2.5V and measuring its output voltage at $V_{BUCK}$ pin. The measured output versus input behaviour across 3 boards is shown in Fig. 6 and the line regulation is measured to be around 75.4mV/V.

Load regulation of the buck converter is measured by varying the load current from no-load (0A) to full-load condition (~1A) and measuring the $V_{BUCK}$ output. The typical load characteristics are shown in Fig. 7. Theoretically, the output of the buck converter should be regulated to 1.5V regardless of the load current. The measured load regulation for three different samples is around 20mV/ΔI. This is higher than the simulated value due to presence of some resistive element in the current path. For example, a 20m□ series PCB trace resistance at the output could also responsible for such a load regulation result.

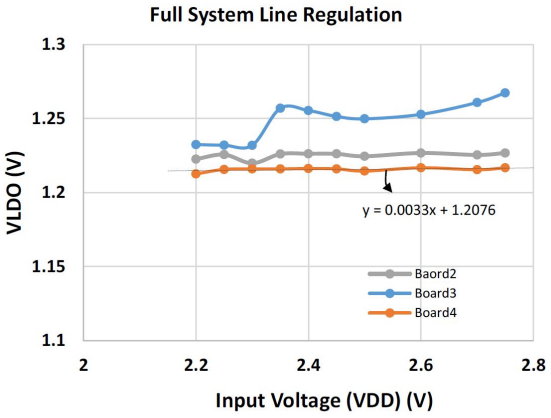


Figure 8. Full System Line Regulation Test

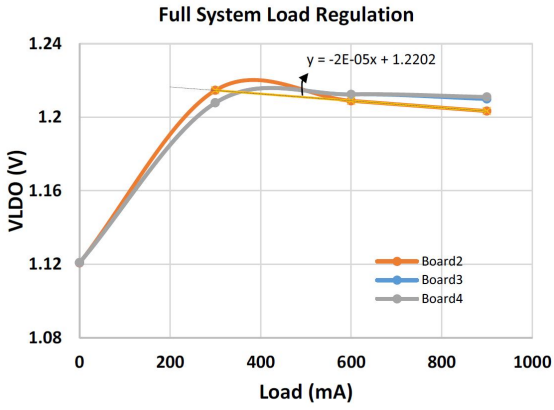


Figure 9. Full System Load Regulation Test

### 4.2LDO Load and Line Regulation

As described in section 1, there is a feature to test LDO as a standalone block. The measurement results of such a block are presented in the reference paper [6].

### 4.3 Full System Tests

The overall power management unit is also characterized for its load and line regulation. The line regulation of the system is obtained by varying the

power supply voltage at VDD pin by 10% around 2.5V and measuring the final output voltage at $V_{LDO}$ pin. The behavior of the full system under different input conditions is shown in Figure 8. The slope or the trend line of the plot gives the quantitative value of line regulation value. The best case measured line regulation as seen from the plot is 3.3mV/V.

Likewise, the load characteristics is obtained by varying the output current while keeping the input voltage same. The behavior of the full system under different output conditions can be observed from the plot shown in Figure 9. The slope or the trend line of the plot gives the quantitative value of load regulation as 20mV/ΔI.

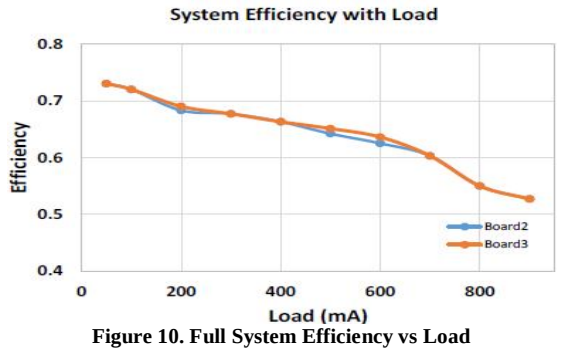


**Figure 10. Full System Efficiency vs Load**

### 4.4 Efficiency Measurements

The efficiency of the overall system is plotted against the load current in Figure 10. The peak efficiency is lower than the buck converter efficiency due to inclusion of an LDO between input and output. The LDO efficiency is determined purely by the ratio of its output voltage and input voltage; and hence is not plotted here.

Table II Summarizes the overall measurement results, obtained for load regulation, line regulation & efficiency.

**Table II: Summary of measurement results**

| Characteristics | Bandgap (Typical) | Buck Only | Full System |
|---|---|---|---|
| Line Reg (ΔV/V) | 0.003 | 0.075 | 3.3 |
| Load Reg (ΔV/ΔI) | -- | 0.02 | 0.02 |
| Peak Efficiency (%) | -- | -- | 73% |

## CONCLUSION

In this paper, a power management unit comprising of a two-stage conversion - buck converter as front-end converter and an LDO as the second stage is presented. The PWM based buck converter provides high conversion efficiency, while the LDO assists in providing tight output voltage regulation and high PSRR. The design is implemented in 130nm CMOS technology node and fabricated. The PMU is verified for converting 2.5V to 1.2V output while having the intermediate buck converter output as 1.5V.

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