AN ADAPTIVE CLOCK GLITCH REMOVAL CIRCUITRY FOR RADIATION-RESILIENT CLOCK NETWORK IN DIGITAL SOC

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Abstract - High-energy environmental radiation particles may affect the operational reliability of a System on Chip (SOC). These particles may cause errors in the combinational logic, sequential logic, and even in the clock network. In the latter, they appear as clock glitches that propagate, and eventually, incorrectly latch all the sequential circuits, such as flip-flops and latches attached to the clock node concerned. The impact on chip functionality is usually fatal. In this work, we propose a low-cost adaptive clock glitch removal circuitry for radiation-resilient clock networks. The proposed technique can be adjusted based on the actual clock glitch profile, to ensure that the error in the clock network is removed, while the impact on the clock signal itself is minimized. It is fully synthesizable, and can thus be incorporated in a conventional digital flow.

Index Terms - Radiation-Resilient, Clock Network, SEU.

I. INTRODUCTION

When microchips operate in a radioactive environment such as outer space or medical equipment, high energy particles from various radiation sources such as cosmic rays may strike certain parts of the semiconductor materials. This phenomenon usually causes two types of errors: Total Ionizing Dose (TID), which results in degradation of the chips performance gradually over a long period of time and, Single Event Effects (SEE), which causes sudden changes in the localized or global behavior of the chips. TID is a long term radiation effect due to trapped high energy particles in the transistors gate. This alters the transistor threshold voltage and causes long-term, irreversible functional shift and leakage current increments. TID is closely related to the gate thickness of transistors. The thicker the gate is, the higher TID will be. It has been found that TID becomes insignificant when the gate oxide thickness is reduced to below 12nm. This corresponds to IC fabrication technologies of below 0.35 μm[1]. Therefore, for modern Deep Sub-Micron (DSM) IC fabrication technologies (e.g. 65 nm, 40 nm), the impact of TID is inherently insignificant. On the other hand, SEE has become increasingly problematic when transistors are scaled into the DSMregime[2], [3]. In addition, the continuous reduction of transistor feature sizes and supply voltages, and the use of increasingly higher operating frequencies, have led toa total reduction in chips tolerance against noises. SEE includes Single Event Upset (SEU) and Single Event Latch-up (SEL). SEL occurs when radiation-induced high energy particles accidentally turn on parasitic transistors in silicon. It causes large DC currents and heat dissipation, which may damage the silicon permanently. SEU occurs when high energy particle hits a certain part of the chips. It usually causes bit flipping in memories (e.g. flip-flop, SRAM), or voltage (or current)glitches in signals in the combinational logic or the clock nodes.

Several circuit techniques have been proposed in dealing with SEL and SEU. In one commonly used method, SEL is reduced by adding guard rings in the circuit layout. For SEU, the use of radiation-resilient flip-flops and SRAM circuits is able to prevent or correct radiation-induced errors which occur inside the flip-flop and the SRAM. However, if the errors occur in the clock network, all of the circuits using the clock will be affected. In fact, errors occurring in the clock network are more serious than errors in the cells, or blocks. Due to the high fan-out nature of the clocking structure, an error in a clock signal is expected to affect many cells or blocks, in different parts of the SOC. The likelihood of an entailing system failure is higher.

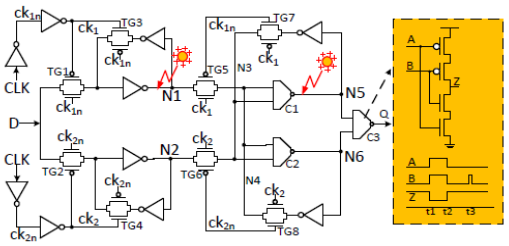

Fig.1. Radiation-resilient flip-flop [1].

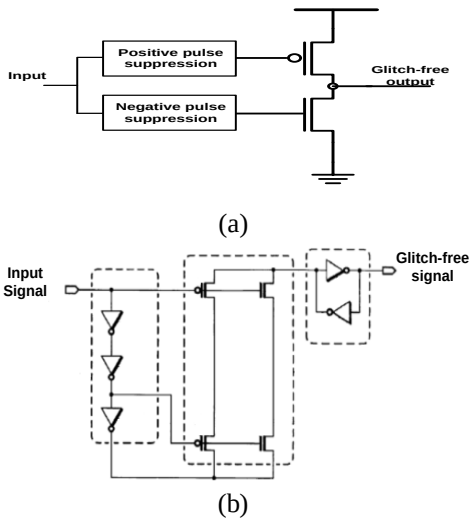

Fig.2. Clock glitch removal circuitries [3], [4].

The radiation-resilient techniques discussed hitherto are suitable for correcting SEU errors that occur inside each individual memory element (i.e. a latch, flip-flop, or SRAM cell). However, if the error occurs in the clock network, it will propagate to all the sequential circuits (e.g. flip-flop, SRAM) that use the same clock signal. This type of errors cannot be easily fixed by the techniques discussed so far. In dealing with the SEU errors that happen in the clock networks, a clock glitch removing technique[3], [4] has been proposed, as shown in Fig.2(a). In this technique, delay control circuits are used to generate delay for clock buffers. The delay can be tuned so that any SEU-induced glitch shorter than the delay cannot propagate to the output of the clock buffer. As the rise and fall delays are separate, two delay control circuits are added to control the pull-up path delay and pull-down path delay respectively. Fig.2(a) shows a simple implementation of this technique while Fig.2(b) shows a more complex version. In Fig.2(b), the delay is achieved by a chain of inverters, and a cross-coupled inverter is added at the output to keep the data. However, the method may have adverse side-effects on the clock networks. To address the issue, we introduce a technique which is low-cost, and amenable to being included a typical digital design flow. With its deployment, the adverse effects of radiation on clock network structures are expected to be mitigated. In the following section, we discuss the existing designs available. Section III details the proposed circuit and implementation. Section IV presents the operation in detail.

II. EXISTING DESIGNS

Many techniques have been proposed in the past to address the issue of SEU errors in digital ICs. For instance, redundant structures with C elements have been proposed to make flip-flops radiation-resilient [1]. As shown in Fig. 1, unlike in a conventional flip-flop, there are two data or clock (data/clock) paths in the radiation-resilient flip-flop. The outputs of the two data/clock paths are merged at a C element. If an error occurs at one of the data/clock paths, the output of the C element will not change. Only when the data/clock at both paths changes, the output of the C element will change.

In this way, the radiation-induced error can be corrected and will not propagate to subsequent circuits. For SRAM, there are also some techniques employed to correct the SEU errors. They include adopting an error correction coding (ECC) scheme and designing the SRAM circuit in such a way that the SEU-induced charge will quickly be discharged. However, both techniques shown inFig.2share a problem when used in removing SEU-induced glitches in the clock network. As the delay is pre-fixed while the glitch information is not known in advance, a short delay may not besufficient to cover the glitch. Or if the delay is too long, it may severely distort the clock signal.

III. PROPOSED TECHNIQUE

Glitches are short pulses in the clock network, generated by radiation particles bombarding the silicon chip. The proposed buffer filters out these short pulses by increasing the intrinsic delay of each clock buffer. Intuitively, if the delay of the buffer is longer than the width of the glitch, it will be filtered out. Based on this reasoning, we propose an adaptive clock glitch removal circuitry for radiation-resilient clock networks, as shown in Fig. 3.Fig. 3(a)

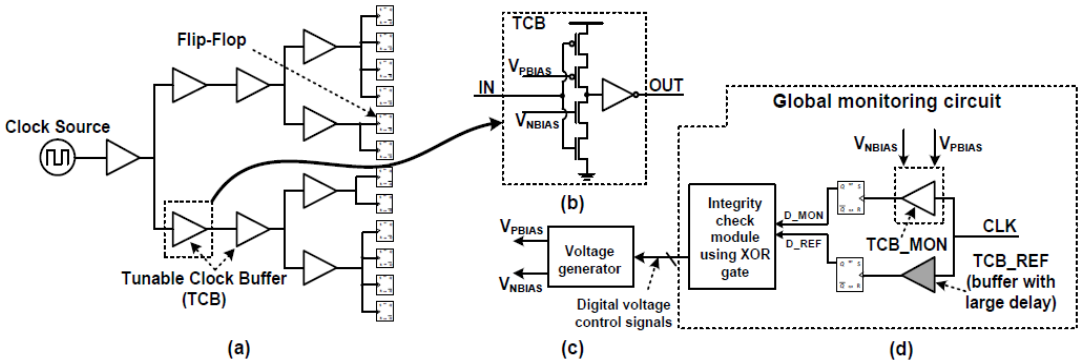

Fig.3. The proposed adaptive clock glitch removal circuitry (a) Clock tree model (b) Tunable clock buffer (TCB) (c) Voltage generator (d) Global monitoring circuit.

depicts a common structure of the clock network. It consists of multiple clock buffers which drive a large number of flip-flops across the chip. In the proposed technique, we replace the type of conventional clock buffer used with a type of buffer called Tunable Clock Buffer (TCB), as shown in Fig.3(b). The difference between TCB and a conventional clock buffer is that TCB has an internal tunable delay inverter. This internal tunable delay is controlled by two bias signals (V_{PBIAS} and V_{NBIAS}). V_{PBIAS} and V_{NBIAS} are shared across the chip and generated by a voltage generation module, also shown in Fig. 3(c). By controlling these signals, intrinsic delay of each clock buffer can be increased adaptively to filter out

glitches caused by radiation events. In the global monitoring circuit, the clock signal from the clock network is fed into two TCB cells: TCB_MON (i.e. "monitoring"), and TCB_REF (i.e. "reference"). TCB_MON shares the same V_{PBIAS} and V_{NBIAS} as TCBs in the clock network, while TCB_REF has its V_{PBIAS} and V_{NBIAS}connected to fixed voltage levels which results inrelatively large delay to make sure that all the glitches are filtered out.The outputs of the TCB_MON and TCB_REF are used to clock two flip-flops as shown in Fig. 3(d). Both flip-flops havetheir inverted outputs connected to the inputs so that the outputs will toggleat every rising edge of the clock signals.

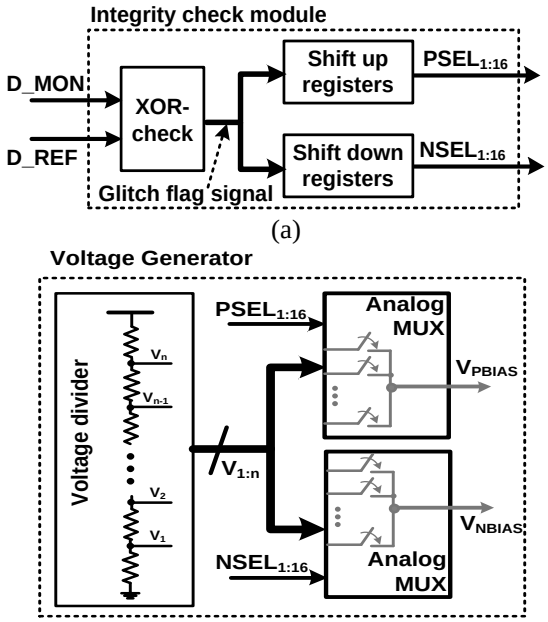

Fig.4.Schematic of the (a) integrity check module and (b) voltage generator.

For the first flip flop which is connected to TCB_MON, the clock rising edgecan be from the actual clock itself orfrom the glitch.For the second flip-flop which is connected to TCB_REF, the clock rising edge always comes from the clock itself, as the TCB_REF's delay is set large enough to filter out any possible glitches. Thus, in the event that glitch happens at the output of the TCB_MON, D_MON changes while D_REF stays that same, causing them to differ. The difference between D_MON and D_REF (i.e. caused by clock glitches)will be captured by the integrity check module (Fig. 3(d)) which generates error pulses (e.g. glitch flag signals)by using XOR gate. Every glitch at the output of TCB_MON will result in an error pulse. When an error pulse is generated, both flip-flops get reset automaticallytoensurethat one glitch willgenerate only one error pulse.The error pulses inthe integrity check module are used to clock the shift registersto produce theappropriate digital control signals to the voltage generator. These digital control signals in turntrigger the change in the controlling word and thus the change of both V_{PBIAS} and V_{NBIAS}in all TCBs, including TCB_MON. In this way, a closed-loop is formed to tune both V_{PBIAS} and V_{NBIAS} of TCBs until the glitch in the clock is removed.

Fig. 4 shows the integrity check and voltage generator in more details. As mentioned, if D_MON and D_REF differs, XOR-check will generate an error pulse (i.e. glitch flag) which clocks the shift-up and shift-down registers. These registers produce the signals $PSEL_{1:16}$ and $NSEL_{1:16}$, respectively. Note that $PSEL_{1:16}$ counts up while $NSEL_{1:16}$counts down.

The voltage generator consists of a voltage divider and two analog MUXs, as shown in Fig. 4(b). The voltage divider can be constructed by cascading N identical resistors in series to produce N voltage levels $V_1 \ldots V_n$. $PSEL_{1:16}$ and $NSEL_{1:16}$from the integrity check module are channeled as inputs to the Analog MUXs, in which one of the voltage levels from V_1 to $V_n$is selected and output as V_{PBIAS} and V_{NBIAS}. $PSEL_i$ is one-hot coded. The same applies for NSEL. For example, if $PSEL_{[3]} = 1$, then $V_{PBIAS} = V_3$.

To evaluate the effectiveness of the glitch removal design pre-silicon, a glitch generator circuit has also been designed to generate and randomly inject glitches to the clock network. As shown in Fig. 5, glitches are observed in the conventional clock nodes but not in the new design.

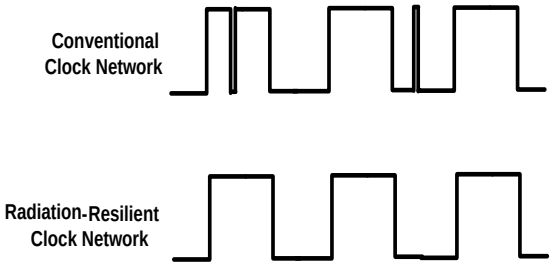

Fig.5. Simulation waveforms.

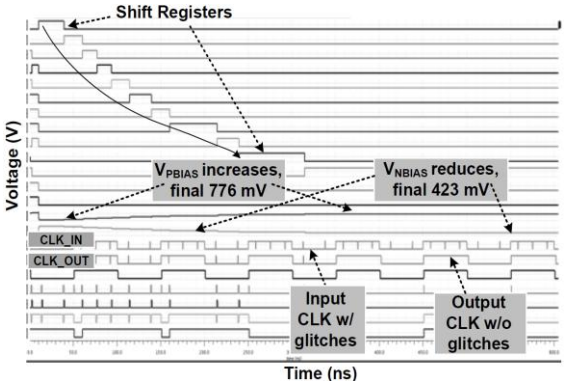

Fig.6.Functional waveforms.

The proposed technique has been implemented using 65nm CMOS technology, and the functional waveformsare as shown in Fig. 6. A glitch generator is used to inject glitches into the original clock signal for verification purpose. At the beginning of theoperation, V_{PBIAS} and V_{NBIAS} are set to 0V and

1.2V, respectively. As glitches are present in the clock waveforms, it triggers the XOR-check, and thus the adaptive tuning of V_{PBIAS} and V_{NBIAS} is initiated. As can be seen in Fig. 6, V_{PBIAS} increases while V_{NBIAS} decreases to increase the buffer delay. Gradually, it reduces the number of glitches by increasing the delay of TCBs. V_{PBIAS} and V_{NBIAS}finally settles down to 776mV and 223mV, and the glitches are completely eliminated. After which, the adaptive tuning is automatically stopped. The proposed technique not only makes sure that the glitches are removed, but also minimizes the impact of the delay on the clock signal.

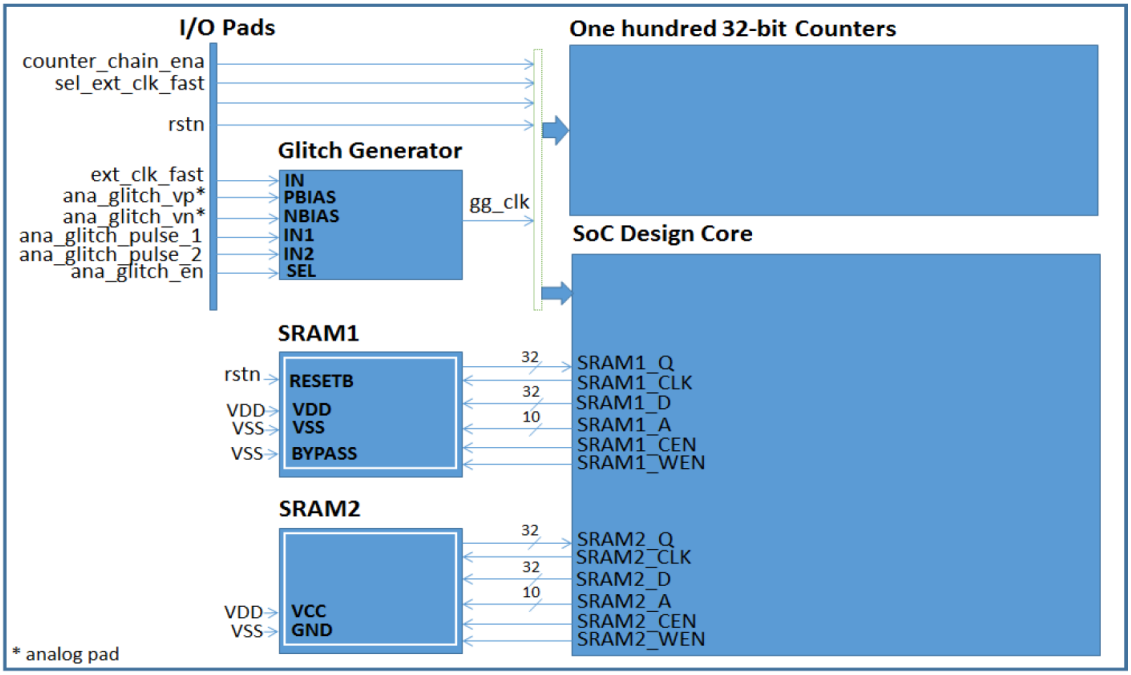

Fig.7. Block diagram of the integrated chip to evaluate the performance of the proposed design.

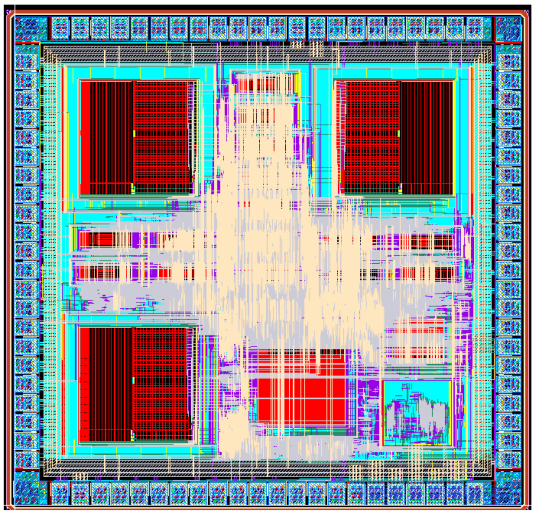

Fig.8.Layout of the integrated chip.

IV. SOC IMPLEMENTATION

We integrated the proposed glitch removal cell into an SoC, the block diagram of which is as shown in Fig. 7. The glitch generator was also included for the purpose of on-chip verification. The design was fabricatedusing a standard low-power 65 nm CMOS process flow. The glitch removal cell and the glitch generator layout were customized to be compatible to theconventional digital placement and routingprocess. The design occupies1.9 mm x 1.9 mm in area, as shown in Fig. 8.

CONCLUSIONS

In this paper we propose an adaptive clock glitch removal circuitry for radiation-resilient clock network to remove the clock glitches induced by radiation. The proposed technique monitors the actual glitch profile and adaptively tunes the delay of the tunable clock buffers to remove the glitch. It is able to ensure that glitches are removed, while minimizing the resulting delay impact on the clock signal.

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