AN ADAPTIVE AREA EFFICIENT SPIN ORBIT TORQUE NON-VOLATILE FLIP FLOP DESIGNWITH HIGH IMMUNITY FOR VDD INSTABILITY

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Abstract - This paper proposes an adaptive spin orbit torque non-volatile flip flop (SOT-NVFF) design. The proposed design offers two schemes of operation to ensure data security. Firstly, the nominal scheme at which the data is stored on the SOT-MTJs only when an external enable signal is initiated. A second scheme is automatically activated when supply instability is detected. This scheme stores the data every clock cycle, which aids in achieving higher data security. The control circuit that switches between the two schemes is also presented in this paper. Furthermore, the proposed NVFF only requires four overhead (OH) transistors, which results in more compact design compared to its counterparts in the literature. It also utilizes a series writing technique that aids in achieving at least 21% lower backup energy compared to others. Further study shows that the proposed NVFF offers better V_{DD} scalability. It is also robustandstable even with process and device variations.

Keywords - SOT, MTJ, NVL, Power Gating

I. INTRODUCTION

Non-volatile flip-flops (NVFF) [1-4]offer a promising solution to eliminate the increasing leakage power consumption issue[3]. NVFFs maintain the data of the leaky idle modules, which permits power-gating (PG) [3, 5]these modules and remove its leakage power contribution. In addition, as the NVFFs are non-volatile, they can also be power gated, which allows further reduction of the overall leakage power consumption [6]. Furthermore, NVFFs may enhance the data security and permit data retrieval in case of sudden power failure.

Data security is essential in certain applications such as military based applications, in which it may even be acceptable to allow a certain higher energy consumption penalty. In that case, the NVFF would be required to contain the most recent data in any case of sudden power supply failure once the power supply is restored. In addition, converting the volatile flip flop (VFF) to be NVFF should be achieved with both low area and energy overheads [3]. The energy overhead (E_{OH}) results from the need for backing up and restoring the data, while the area overhead is due to the required additional circuitry to achieve non-volatility.

An SOT-MTJ, depicted in Fig.1, comprises an MTJ and a HM electrode. The MTJ consists of apinned magnetization ferromagnetic (FM) layer(PL), free magnetization FM layer (FL), and an oxide barrier in-between. The magnetization of the FLchanges to be in parallel (P) or anti-parallel (AP) directions to the PL to form low resistance state or high resistance state, respectively.

Utilizing magnetic tunnel junctions (MTJs) in NVFFs is a viable solution due to the various advantages of the MTJs such as its non-volatility, CMOS process compatibility, high endurance, 3D stacking capability and long state retention time. In addition, energy efficient writing technologies for the MTJis available such as such as spin-orbit torque (SOT) technology

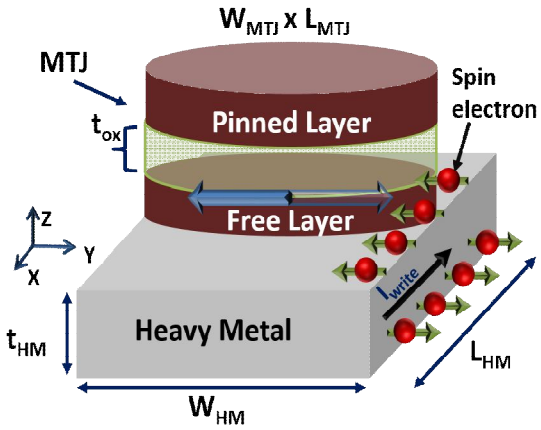


Fig. 1 Spin-orbit torque magnetic tunnel junction (SOT-MTJ). [2, 7, 8].

The FL of the MTJ is placed in contact to the HM electrode. The FL magnetization(m_F)is switched to one of thetwo states through supplying a current in the HM greater than certain critical current (I_c). The current flowing in the HM electrode causesaccumulation of spin electrons in the MTJ's free layerdue to the spin-orbit interaction. The accumulated spin electrons cause the change of the $m_F$to P or AP state based on the direction of the supplied charge current. The SOT writing technology can result in high speed and energy efficient switching thanks to the large spin injection efficiency, where the injected spin current can be larger than the programming charge current. Furthermore, the write current flow through the low resistance HM electrode,

which reduces the write path resistance and enhances the device reliability. Thus, the SOT-MTJ can be utilized to achieve both energy and area efficient NVFF (i,e, SOT-NVFF).

The existing SOT-NVFFs architectures in the literature do not properly address the data security and immunity to V_{DD} instability. In addition, few drawbacks exist in the various

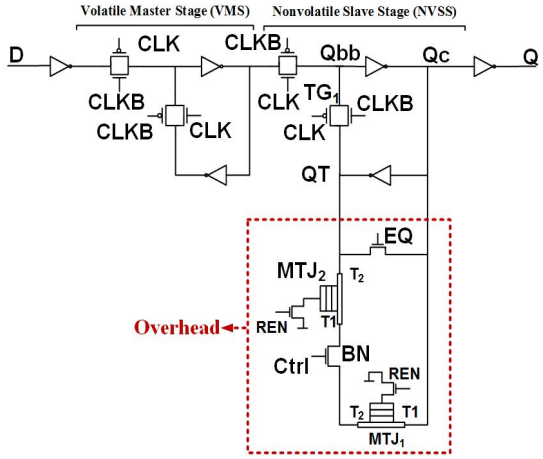


Fig. 2Proposed SOT-NVFF schematic.

designs that result in large area overhead or high energy consumption. In [1], the write path resistance is large as the result of the presence of two transmission gates (TG) in-series and a tri-state inverter while storing the data on the SOT-MTJs. This causes a write current degradation and increases the energy consumption. The design also employs ten OH transistors. In [2], the write current is degraded by the TG in the latch loop, which results in higher energy consumption. In addition, a parallel writing technique is employed, which needs doubling the generated write current [4].Moreover, it requires five OH transistors.In [4], we proposed an area and energy efficient SOT-NVFF. The proposed NVFF requires only four OH transistors. It also employs series writing technique that aids in achieving low energy consumption. However, in all these designs, the data is only stored on the MTJs when an external enable signal is exerted before the initiation of the standby mode. This may result in data loss in the duration of the power supply instability and sudden power failure.

Hence, in this paper, an improved design with two schemes of operation for the SOT-NVFF is proposed. A nominal scheme (NS) at which the data is stored on the MTJs only when an external enable signal is exerted. A data security scheme (DSS) that stores the data on the MTJs every clock cycle. The switching between the two schemes occurs by only controlling the input signal to one transistor, which aids to reduce the load on the control circuitry. In addition, the paper also presents the control circuitry required to switch between the two schemes. The paper is organized as follows: Section II demonstrates proposed NVFF. The control circuitry to switch between both schemes is illustrated in Section III and the evaluation is presented in Section IV. Finally, Section V concludes the paper.

II. PROPOSED NON-VOLATILE FLIP-FLOP (NVFF)

Fig.2 presents the proposed NVFF, which is composed ofa conventional volatile static flip flop (VFF), two always complementary SOT-MTJs and four overhead transistors. The four OH transistors and the two SOT-MTJs convert the VFF to be NVFF. The proposed NVFF can be employed as either a master stage or a slave stage in a master-slave flip flop to implement the NVFF, while the other stage would be the conventional VL. The back-to-back inverters in the VL is used for both reading and writing the SOT-MTJs in order to reduce the area OH [4]. The proposed SOT-NVFF can operate with two different schemes based on the control circuitry decision, which drives the Ctrl signal. The two schemes are a nominal scheme (NS) that stores the data on the MTJs following an external backup-enable (BEN) signal and a data security scheme (DSS) that stores the data on the MTJs every clock (CLK) cycle. In both schemes the NVFF would have different possible modes of operation as discussed in the following.

A. Nominal Scheme (NS)

The nominal scheme is activated once the control circuitry decides that the power supply is stable. In this scheme, the Ctrl signal follows an external backup enable signal (BEN) and the data is stored on the MTJs only when the BEN signal is high,mainly before switching from active mode to sleep mode, where in the sleep mode the different modules are power gated. Hence, four different modes of operations exist in this scheme, which are active, backup, sleep and restore. In the active mode, the FF follows the same nominal behavior of a VFF at which Q=D when the CLK signal is high. Moreover, both the REN and Ctrl (BEN) are set low such that the SOT-MTJs becomes float and does not intervene with the VFF functionality. Thereafter, in case the modules are going to be in an idle state (i.e. sleep mode) the FF current stateisfirst saved on the SOT-MTJs while being in the backup mode. In the backup mode, the Ctrl (BEN) signal is set high and a write current is generated from the internal latch (i.e. back-to-back inverters) to program the two SOT-MTJs as depicted in Fig.3(a). The write current (I_{write}) direction varies with the input data 'D' value. To back-up a '1', the I_{write} flows from Mp2 to Mn1, as highlighted in Fig. 3(a), whereas to store a '0' the I_{write} flows in the opposite direction from Mp1 to Mn2. The generated write current programs the two MTJs in complementary states. Furthermore, the REN signal is pulledlow to guarantee that the read transistorsconnected to the MTJs are off and no current pass by the MTJs. Then, in the sleep mode,

the NVFF and the corresponding modules can be power gated while the data are maintained on the non-volatile MTJs. It is required to activate the restore mode before returning to active. In the restore mode, the stored data in the MTJs are restored to the VFF by setting the REN signal high and the Ctrl low. The internal latch is used to sense the state of the two MTJs as presented in Fig. 3(b) and discussed in [4].

B. Data Security Scheme (DSS)

The data security scheme is activated, once the control circuitry decides that the power supply is unstable and there is a high chance of sudden power supply failure (i.e. data loss). In this scheme, the Ctrl signal follows the system CLK, which means the data are stored on the MTJs every CLK cycle within the CLK 'high' duration. Hence, only three modes of operation exist in this scheme, which are active, restore and sleep. In the active mode, the NVFF still behaves as normal VFF at which Q=D when the CLK signal is high. Simultaneously, a write current flows through the branch comprising the two SOT-MTJs to program the MTJs with the data existing in the latch, as illustrated in Fig. 3(a). The REN signal is kept low in order to prevent any current from flowing through the MTJs. It is worth mentioning that, in this scheme,

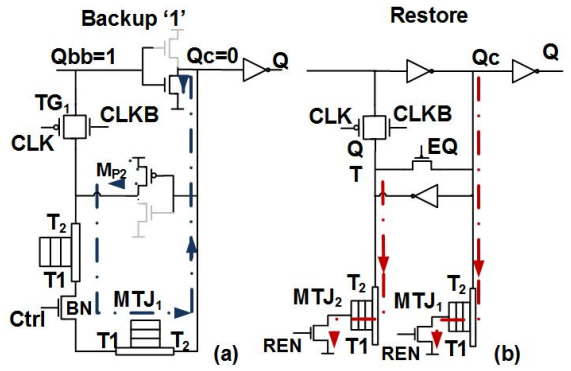


Fig. 3 NVFF configuration in the (a) backup mode (Q = '1'), (b) restore mode respectively. The current flow direction is also indicated in the figures.

the CLK 'high' pulse duration should be long enough to satisfy the required timing for programming the SOT-MTJ at the supplied write current value. Hence, in this scheme, the CLK speed is limited by the SOT-MTJ technology switching time. Furthermore, the active energy consumption is relatively larger compared to the nominal scheme due to the additional energy consumption to write the SOT-MTJs.

As the data is stored on the MTJs every clock cycle, the FF becomes more immune to sudden power failure and data loss. Moreover, anytime the modules are idle, both the modules and the NVFF can be power gated to eliminate their leakage contribution, which is the sleep mode for the NVFF. To resume the normal operation after being in the sleep mode, the data needs to be first restored to the FF during the restore mode. The restore operation in this scheme is identical to that of the nominal scheme, where the REN signal is set high and the CLK is low. The circuit configuration in this mode is as shown in Fig. 3(b) and its operation is discussed in [4]. It is noteworthy that, in this scheme, the backup mode is no longer needed as the data storing occurs in the active mode.

III. CONTROL CIRCUITRY

The decision to switch between the two schemes requires a proper control technique that decides the appropriate time to move from the lower active energy nominal scheme to the higher active energy data security scheme based on the status of the power supply. The control system can be simply presented as depicted in Fig. 4(a), which is composed of a power supply instability detection unit and a decision unit. The Instability Detection Unit (IDU) detects whether or not the power supply is stable. Thereafter, the IDU modifies the 'Mod' signal in the Decision Unit (DU) in order to choose whether the Ctrl signal is equivalent to the external backup enable signal (BEN) (i.e. nominal scheme (NS)) or the CLK signal (i.e. data security scheme (DSS)). The IDU can be implemented simply as a comparator, which compares the current V_{DD} level and a certain V_{DD_limit} value at-which the V_{DD} is considered critically low. However, in that case, a sudden change in the V_{DD} to the V_{DD_limit} results in switching from the NS to the DSS, which might not be needed and results in higher energy consumption. Another

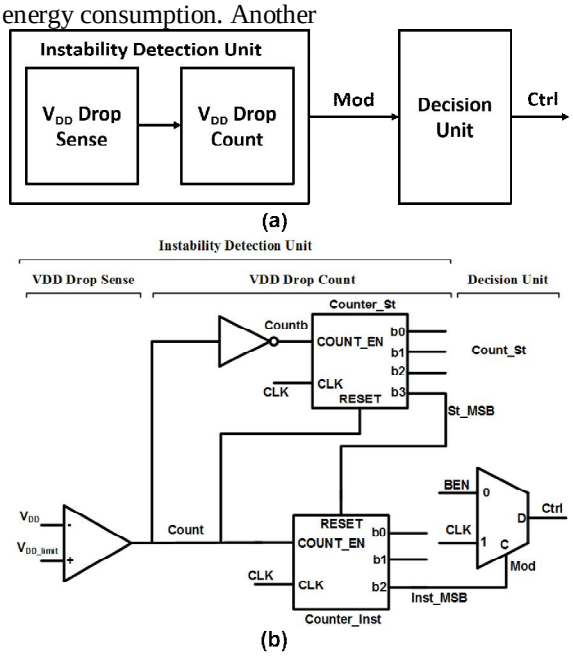


Fig. 4 (a) Generic block diagram for the required control circuitry to switch between the two schemes. (b) An implementation for the control circuitry.

approach is to include a V_{DD} drop cycle counting module in addition to the V_{DD} drop sense (i.e. comparator) as shown in Fig.4(b). The V_{DD} drop cycle count module ensures that the V_{DD} supply is at or below the V_{DD_limit} for certain number of cycles instead of just a sudden change before raising the flag to switch to the DSS. Using the implementation depicted in Fig.4(b), the control circuitry operates as illustrated

in the flowchart in Fig.5. The instability detection occurs as follows: firstly, the comparator outputs a count='1' in case $V_{DD} \leq V_{DD_limit}$. Once the 'count' signal is raised high, it enables incrementing the current value of the counter_inst by one. In addition, it resets the value of the counter_st to 0. Resetting the counter_st ensures that any sudden occurrence for a $V_{DD}>V_{DD_limit}$case within instability cycles counts would be ignored. Once the counter_Inst reaches the Count_Inst_lim,the Inst_MSB switches from '0' to '1', which mean the Mod signal becomes '1' and the DSS is activated (i.e. Ctrl=CLK). The DSS would be operational till the VDD level goes back to normal levels ($>V_{DD_limit}$)for multiple cycles. In each cycle the V_{DD} is greater than $V_{DD_limit}$the comparator output signal count='0'. Thus, the Counter_St enable signal is high and its value is incremented by one. After certain stable cycles, depending on the counter size (i.e. seven cycles for 4-bit counter), the St_ MSB switched from '0' to '1' as the count reaches Count_St_lim. This reset the Counter_Inst to '0', which results in Inst_MSB ='0' (i.e. Mod='0') and the NS is reactivated (i.e. Ctrl=BEN). The size of both Counter_St and Counter_Inst determine the delay to decide the change of the system state from unstable to stable and vice versa, respectively and it would depend on the application nature. It worth mentioning that both counters are designed such that

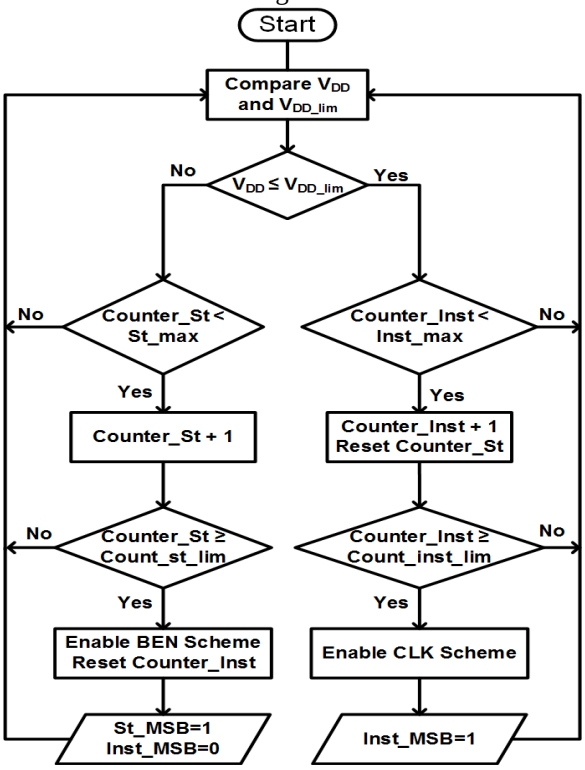


Fig. 5 Flowchart of the proposed control circuit shown in Fig.4(b). V_{DD_limit} is VDD level at which instability is expected. Counter_St and Counter_Inst is the current value of both the stability (top counter in Fig. 4(b)) and instability (bottom counter) counters, respectively. St-max and Inst_max are the maximum values that can be reached by both stability and instability counters, respectively (i.e. 111 for 3 bit counter and 1111 for 4 bit counter). Count_st_lim and Count_inst_lim are the counters values at which the MSB switches from 0 to 1 for both stability and instability counters, respectively (i.e. 100 for 3 bit counter and 1000 for 4 bit counter).

once the counter max value (St_max or Inst_max) is reached it would not revert back to '0'.

IV. EVALUATION

In order to verify the proposed SOT-NVFF, the SOT-MTJ Verilog-A modelpresented in [4] is employed, with parameters shown in Table I. Moreover, a 45nm technology node is employed and the simulations run over Cadence. The simulated waveform for the proposed NVFF with the control circuitry is depicted in Fig.6. Firstly, the NVFF operated in the NS (i.e. Mod='0'), where the Ctrl signal follows an external BEN signal. Thereafter, as the control circuitry detect supply instability as described in Section III, the Mod signal change to '1' to activate the DSS and the Ctrl follows the CLK instead of the BEN in order to back up the data on the MTJs every CLK cycle.

TABLE I. PARAMETERS OF EMPLOYED SOT-MTJ.

Symbol	MTJ Parameter	Value
W_{MTJ} x L_{MTJ}	MTJ Dimensions (WxL)(nm^2)	50x100
K_u V / KT	Thermal Stability	46
t_{MgO}	Tunnel Barrier Thickness (nm)	1.5
t_{HM}	Heavy Metal Thickness (nm)	3.3
W_{HM}	Heavy Metal Width (nm)	120
Ms	Magnetization Saturation (emu/cm^3)	1114
R_{AP}	High Resistance of MTJ value (kΩ)	22
TMR	Tunnel Magneto-resistance Ratio (%)	83
θ_{SHE}	Spin Hall Angle	0.3

As depicted in Table II, our proposed NVFF requires only four OH transistors, which results in more compact design compared to others in the literature. In addition, our proposed design in both schemes employs series writing technique that aids in achieving lower writing energy consumption compared to other writing techniques as illustrated in [3][4].The restore energy for both schemes is 6 fJ within the duration of 80 ps. In the NS, the backupenergy and active energy are 388 fJ and 35fJin duration of 4.95 ns and 0.5 ns, respectively. Whereas in the DSS, the backup and active energy are combined in the active mode to results in a higher active energy consumption of 378 fJ as a result of storing the data on the MTJs every CLK cycle. This higher active energy can be an acceptable penalty for the additional data security feature in applications such as the military based ones. In addition, the table shows further differences between the two schemes. Firstly, the DSS can achieve larger write current compared to NS as TG_1 is turned off (CLK='1') in DSS during the data backup. Secondly, C-Q delay of DSS is 28% faster than NS due to the existence of the resistive path through the HM electrodes while writing in the DSS. This path aids in speeding up the switching when the latch state changes from the previous data. However, that does not actually benefit the latch performance as the CLK speed is still limited by the SOT-MTJ switching time. Further development in the SOT-MTJ switching speed (to be in the ps

range) will result in getting the actual performance benefit in the DSS and would permit reducing its active energy extensively, which aids in widening its application window.

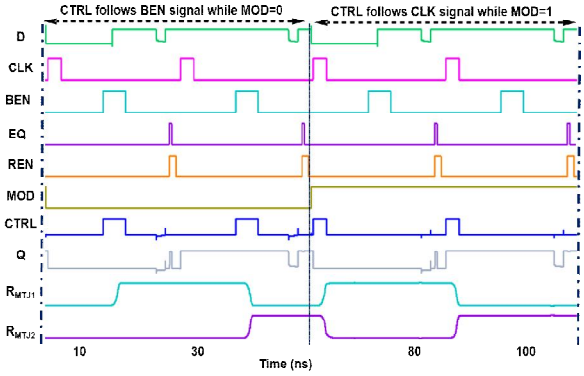


Fig. 6 Simulation of the proposed SOT-NVFF with control circuitry.

TABLE II. VARIOUS SOT-NVFFS COMPARISON.

		Prop. NVFF	Prop. NVFF	[1]	[2]	[4]
Energy (fJ)	Active	378* 338**	35	35	35	35
	Backup	-	388* 347**	427*	854*	835*
	Restore	6	6	6	6	6
Delay (ns)	Active	4.5* 8.9**	0.5	0.5	0.5	0.5
	Backup	-	4.95* 8.9**	8.9*	8.9*	8.1*
	Restore	0.08	0.08	0.08	0.08	0.08
I_{write} / SOT-MTJ		71* 40**	66* 40**	40*	40*	43*
C-Q delay (ps)		26	36	58[a]	36	36
Scheme		DSS	NS	NS	NS	NS
Writing Scheme		Series	Series	Series	Parallel	Parallel
OH Transistor #		4	4	10	5	5

*At V_{DD}=1.2 V, ** At V_{DD}=0.95V
a. Large C-Q due to the existence of extra Mux. delay and the HM resistive path oppose the latch state transition.

Table II also compares various state of the art NVFF designs in the literature with our proposed SOT-NVFF. To guarantee a fair comparison, all the benchmarked designs employ the internal latch to write the SOT-MTJs and the SOT-MTJ technology in [7] is employed in the different designs. As discussed previously, our design does offer a DSS scheme that improves the immunity to power supply instability and sudden power supply failure. On the other hand, none of the designs in the literature has the data security scheme feature in their design in addition to the nominal power gating scheme. Furthermore, our proposed design offers at least 21% less backup energy consumption at equivalent write current and delay compared to other designs. This is thanks to the usage of series writing technique instead of parallel compared to [2] and the parallel design in [4]. In series writing, the write current needs to flow in one branch instead of two branches in the parallel technique[3]. In addition, the lower backup energy consumption compared to [1] is due to the reduced write current path effective resistance, which allows supplying similar write current at reduced VDD. The series writing technique permits our design to be functional at lower supply voltages compared to others [2], [4]as shown in Fig. 7. This is because the total write current required to be supplied to program the two SOT-MTJs is approximately half of that required to be supplied by parallel writing technique.

The robustness of our proposed design is validated by running both Monte-carlo and corner simulations. The corner simulations presented in Table III show that both schemes are functional at the different corners as meta-stability condition is avoided [4], and I_{write} greater than the critical write current (i.e. 21 µA in this design example) can be supplied. In addition, from the 5000 runs of Monte-Carlo simulations, distribution for MTJs magnetization, Q_T and Q_C depicts the preservation of the correct state throughout all the runs during both the storing and restoring of the data. In addition, the I_{write} distribution, with the mean (μ_{Iwrite}) =71 µA and standard deviation (σ_{Iwrite}) = 2.2 µA for DSS (μ_{Iwrite} =66µA and σ_{Iwrite} = 1.9 µA for NS), indicates that our NVFF can achieve up to 6σ variations [4]. It is worth to mention that our designs stability depend on the sizing of the BN transistor and the employed HM resistance, where the resistance between the nodes Qc-QT should be high

TABLE III. PROPOSED SOT-NVFF CORNERS RESULTS.

Corner	FF	FS	TT	SF	SS
DSS					
Write Current (µA)	84.5	73.8	71	68.8	57.7
Switching Delay (ns)	3.99	4.4	4.5	4.75	6
NS					
Write Current (µA)	79.5	69	66	64.8	54.8
Switching Delay (ns)	4.2	4.7	4.95	5.1	6.5

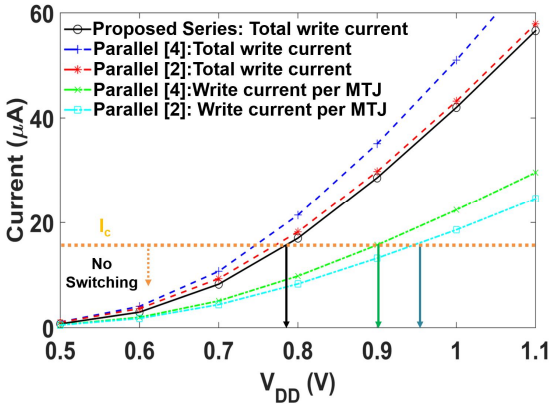


Fig. 7 Voltage scaling comparison between the different designs.

enough to avoid latch meta-stability condition (i.e. data loss) while storing the data on the MTJs.

CONCLUSION

A compact spin-orbit torque non-volatile flip flop (SOT-NVFF) design is proposed in this paper. This design offer two schemes of operations: a nominal scheme (NS) that stores the data on the MTJs only when an external enable signal is exerted and a data security scheme (DSS) that permits storing the data on the MTJs every CLK cycle. The DSS scheme aids in increasing the immunity to power supply instability and sudden power supply failures.Both schemes are easily configured by controlling the gate of a single transistor. The control circuity to switch between the

two schemes is also presented and discussed in the paper. In addition, the proposed design does require only four OH transistors and employs a series writing technique while storing the data on the SOT-MTJ, which permits achieving both more compact and energy efficient writing compared to other design in the literature. The analysis also shows that the proposed design is still functional at smaller supply voltages compared to others, thanks for the employed series writing technique.

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