FAULT TOLERANCE IMPROVEMENT OF THE SECURED CIRCUITS

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Abstract- One of the major problems in testing a system-on-chip is dealing with the optimal choice of the test sequence. In this paper, we propose an efficient test sequence for TMR secure circuits. The test sequence is a high level method based on three pulsations. An extension to the sequence with one pulsation is proposed and by simulation results its effectiveness in achieving a higher fault tolerance interval is demonstrated.

I. INTRODUCTION

The rise of nanotechnology requires the development of reliable test and fault tolerance techniques to address potential risk assessments and post-manufacturing control. Indeed, with the advent of submicron technologies, some physical phenomena that previously were negligible become preponderant. We can mention in particular the variation of the parameters of the transistors (dimensions, doping), the leakage currents due to the variation of the supply voltage and the temperature.

These phenomena that can lead to failures have a direct impact on reliability and manufacturing efficiency. Therefore, achieving higher reliability can only be achieved through extensive testing of integrated circuits and systems. Much work has focused on different methodologies for testing integrated circuits [1-7]. To effectively test an integrated circuit, it is imperative to define fault models in line with the actual defects of current CMOS technologies and future technologies.

Open-circuit defects are the predominant types of manufacturing defects [8]. Previous models of these faults include logic fault and delay fault models, but ignore the resistance of the fault. Most models of resistive open faults [9-11] are used to describe resistive open circuit faults. It is important to note that the resistance of these two faults is an unknown random parameter because it depends on the geometric technological parameters of the fault.

Due to recent technological advances, the secure circuits implemented in WDDL and in QDI countermeasures appear more interesting than synchronous circuits, mainly to secure the implementation of integrated circuits against attacks by fault injection and power analysis. However, the lack of method and test tool has limited the use of this type of circuits.

The objective of this paper is to present a sequence test for improving the fault tolerance of these secure circuits.

We have previously shown that the fault models applied in conventional CMOS structures are also applicable for secure structures fault tolerant, and as these structures can function correctly despite the presence of the two resistive-bridge defects [12] and two resistive-open defects [13]. The various measures are carried out under Spice Cadence. The current paper extends our foregoing activity by employing a more realistic test sequence with n pulsation instead of simply sequence test with one pulsation. The remainder of the paper is structured as follows. Section 2 describes the detection and fault tolerance method. Finally, the results are the aim of Section 3 and Conclusions are detailed in Section 4.

II. DETECTION AND FAULT TOLERANCE

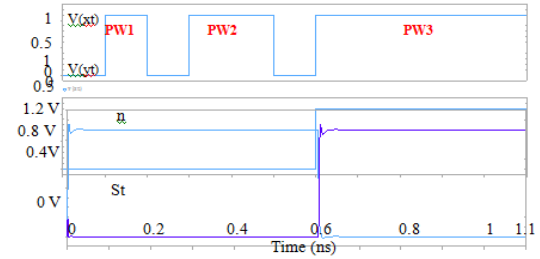
In order to improve the fault tolerance of TMR secure circuits we have used the same tailored method for testing and fault tolerance presented in [13]. So, after injecting the type of resistive open faults at the level of WDDL and QDI AND gates, we will observe and analyze its electrical behavior in order to evaluate robustness and therefore the fault tolerance of these two TMR secure designs.

III. RESULTS OF THE DETECTION WITH A REAL SEQUENCE TEST

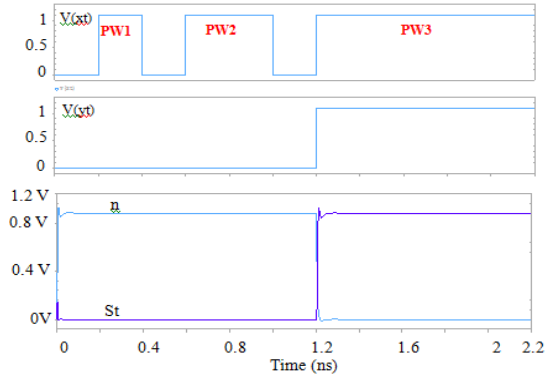
The objective of these simulations is to improve the previous test sequence applied only with a single pulsation [13]. We study the defect detection when it has been tested with a real test sequence. We considered a cycle time of about T_{pulse} = 0.1 ns for the TMR AND WDDL and of T_{pulse} = 0.2 ns for the TMR AND QDI. From an initial pulse given by PW_1, a complete test sequence of i pulsations is applies to the TMR secure circuits. In our case, we will try to detect both open circuit defects with a test sequence witch composed of three different pulse widths [PW_1, PW_2, PW_3]. The test sequence consists of two phases. The phase before the detection: the transition created by the pulsations [PW1, PW2] crosses the nodes n1, n2 and n3, but these transitions do not propagate to a primary output, i.e. the fault cannot be detected. The detection phase: the fault can be detected at the application of the sequence corresponding to PW3.

3.1 Fault-free behaviour simulation

The dynamic behavior of both fault-free TMR is shown in Figure 1. It can be seen that in the case of the two fault-free TMR simulations have the same dynamic behavior. The transitions occur at the arrival of the rising edge of the third pulse PW3 and therefore the TMR function correctly.



a. TMR AND WDDL



a. TMR AND QDI

Fig.1. Fault free behaviour with three pulsations

3.2 Dynamic behaviour simulation of faulty TMR

The behavior of the two defective TMR in the case of different fault resistances is shown in Figure 2. The signals are slowed down by the presence of the two resistive open faults. In TMR AND QDI, faults are detected during PW3. When the PW3 sequence is applied, a transition propagates from the input signals xt and yt to the nodes n, this transition is slowed down by the defects and finally propagates to the outputs St2 and St3. The two defects are detected since the outputs S_t transits just after the rising edge of the third pulsation corresponding to the sequence [xtyt] = [11]. The minimum critical resistance is equal to 19 kΩ in the TMR AND QDI (Fig. 2a). The final voltage of the phase before detection (V_{bd}) is equal to 1.05 ≈ V_{DD}, which is the best fault detection condition with minimal critical resistance. The dynamic behavior associated with resistances below 19 kΩ is insensitive to the presence of both faults and therefore the TMRs are tolerant and reliable. On the other hand, the behaviors associated with resistances higher than 19 kΩ are very sensitive to the presence of defects. In other words, we see that the defective nodes n2 and n3 are only observable on the output signals S_{t2} and S_{t3}. Therefore, a logic error and a malfunction are observed at the output S_t during the sequence = [11]. The test sequence with three pulse widths (PW3) leads to a higher critical resistance than that obtained with the single-pulse test sequence (PW1).This observation with three widths of pulsations has made it possible to highlight a simple technique that involves finding wider tolerance intervals and thus increasing reliability. In the TMR AND WDDL (Fig. 2b), the value of the critical resistance also depends on the pulsations applied because the defects are detected by the third pulse (PW3) corresponding to the sequence [xtyt] = [11]. The value of the minimum critical resistance found is 8.75 kΩ. The potential V_{bd} is equal to 1, 1 V = V_{DD}. It is also shown that the R_C value is lower than that found in TMD AND QDI, which demonstrates once again that TMR AND QDI is more robust than TMR AND WDDL.

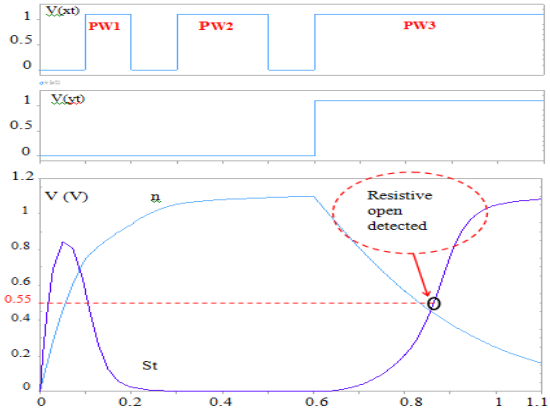
The detection interval (DI) and the tolerance interval (TI) are defined below:

For TMR AND WDDL:

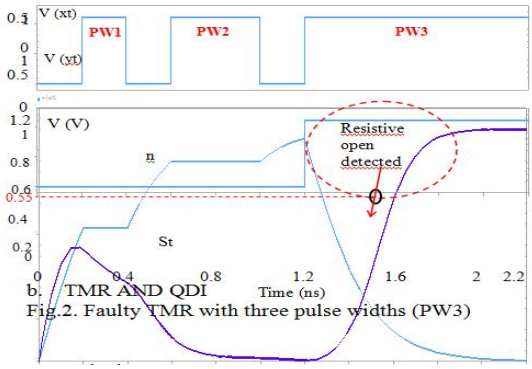
$$DI^{\{PW1,\ PW2,\ PW3\}} = [R_C, \infty [$$
$$= [8.75\ k\Omega, \infty [$$
$$\Rightarrow TI = [0, 8.75\ k\Omega [$$

For TMR AND QDI:

$$DI^{\{PW1,\ PW2,\ PW3\}} = [R_C, \infty [= [19\ k\Omega, \infty [$$
$$\Rightarrow TI = [0, 19\ k\Omega [$$



a. TMR AND WDDL



b. TMR AND QDI

Fig.2. Faulty TMR with three pulse widths (PW3)

CONCLUSION

In this work, we have proposed an extension to the recently proposed sequence test with one pulsation. The proposed technique is based on three different pulsations (PW3) as opposed to the one pulsation (PW1). Based on the simulation results on TMR

secure circuits, it has been demonstrated that the proposed PW3 sequence outperformed the PW1 sequence and resulted in significant increase in the critical resistance of detection, improving the fault tolerance interval from [0, 5.325 kΩ [to [0, 8.75 kΩ[for the TMR AND WDDL and from [0, 5.713 kΩ [to [0, 19 kΩ[.

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