LOW VOLTAGE CCII TECHNIQUES COMPOSITE TRANSISTOR AND BULK DRIVEN

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Abstract- To proof low voltage techniques are valid in current conveyor design, Bulk driven and composite transistor (self cascode) techniques are used to get high performance results from CCII in low voltage supply. Conventional operational amplifier circuit from literature was our choice as core of the design. Our Focus with using low voltage techniques is study the frequency characteristics of a CCII based miller compensated operational amplifier. Orcade 9.2 and 0.7 μm CMOS process model from AMIS used for simulation.

Keywords- Self Cascode; Bulk Driven; Low Voltage Current Conveyor; CCII; Current Conveyor Techniques.

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I. INTRODUCTION

The current-mode approach is voltage mode alternative to obtain high performance architectures, the most advantages of current mode is higher gain bandwidth product. In this work design and construct low voltage second generation current conveyor, their performance are discussed here with corresponding to current frequency response, input and output impedances, dynamic range, finally a comparison with the conventional techniques has been presented.

II. LOW VOLTAGE TECHNIQUES

A. Conventional Design

CCII based Miller compensated two stage operational amplifier shown in figure 1. M1 and M2 perform the voltage following action between Y and X nodes; a feedback connection at X node provides the low impedance terminal.

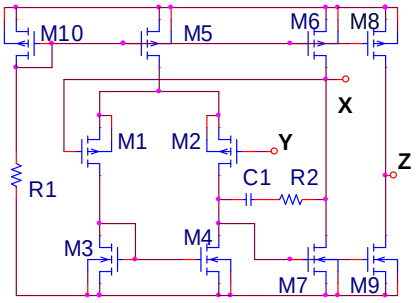


Figure1. CCII- based on the Miller compensated op amp.

M6 and M7 are sensing Input current ix and copied it as output current iz using transistors M8 and M9. Since M8

and M9 have the same size and biasing of M6 and M7, the current iz should be a copy of current ix. It will be shown that the current conveyor formed in this way still have the same characteristics of the core operational amplifier a good voltage follower at the cost of lower bandwidth.

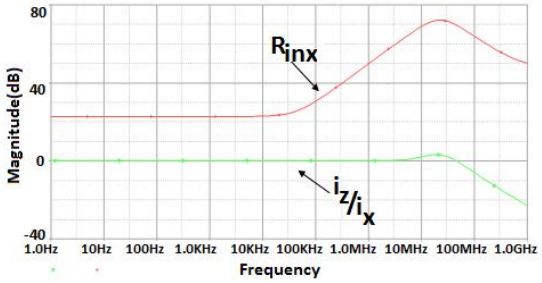


Figure 2. simulation of iz/ix and rin,x, in dB is normalized to 1 ohm

Figure. 2 shows the simulation of the current conveyor based Miller compensated two stage operational amplifier in terms of the current transfer ratio iz/ix and the input impedance of the X terminal rx. The current transfer ratio stays at 0dB indicating the value of | iz/ix | to be unity until approximately the unity gain bandwidth is reached.

B. CCII Based Composite Transistor Op. Amp.

Short channel MOSFETs cannot provide high gain structures due to Channel length modulation. To have high output impedance and thereby high gains, cascoding by composite transistors is done, the regular cascode structures are avoided as their use increases the gain of the structure, but decreases the output signal swing. Composite transistor is the technique which does not require high voltages at output nodes. It provides high output gain due to high output impedance and so it is useful in low-voltage design.

The equivalent output impedance of the composite transistor as expressed in equation 1.

$$r_o = g_{m2} r_2 r_3 - r_2 - r_3 - \approx (g_{m2} r_3 - 1) r_2 = (m g_{m1} r_1 - 1) r_2 = (m - 1) r_2 \quad (m > 1) \qquad (1).$$

It is obvious from equation 1 output impedance of composite transistor is bigger than of conventional, which is most one important feature are demanded in CCII.

The proposed structure diagram of CCII composite transistor miller op-amp is shown in Figure 3, composite transistors can replace single transistors in a differential pair. The gates of transistors M1a, M2a are connected together, the gates of transistors M1b, M2b are connected too to implement composite transistor structure, with the same value approximately of voltage supply that have used in conventional CCII miller op-amp

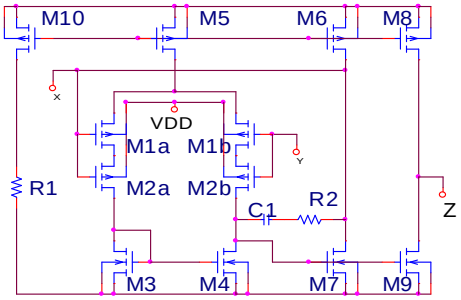


Figure3. self cascode CCII based miller compensated op amp

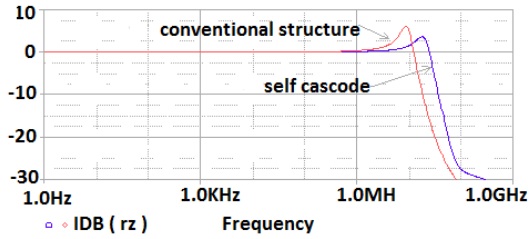


Figure 4. Current transfer for conventional and self cascode

Simulation shown in figures 4 - 6 affirms presented results in table 1, the main advantage Obvious in figure 6 that the dynamic range extended to considerable value.

Characteristics formulas of the previous circuit are:

$$\frac{iz}{ix} = \frac{g_{m8} + g_{m9}}{g_{m6} + g_{m7}} \qquad (2)$$

$$rx = \frac{2}{g_{m1a} r_o (g_{m6} + g_{m7})} \qquad (3)$$

$$rz = \frac{r_{o8} r_{o9}}{r_{o8} + r_{o9}} \qquad (4)$$

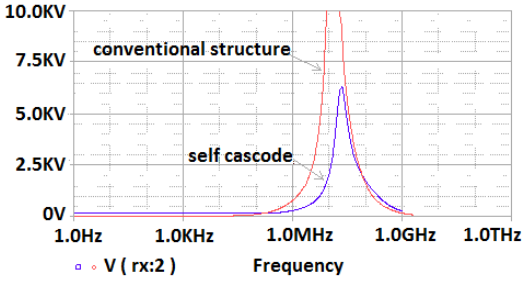


Figure 5. x node impedance for conventional and self cascode

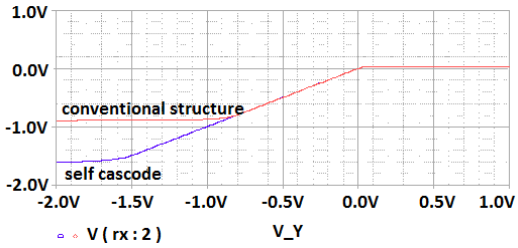


Figure 6. x node and y node voltages

C. CCII Based Bulk-Driven Miller Op Amp

Figure 7 illustrates the input signal is applied to the bulk terminal of the input transistors, M1 and M2 while the gate terminals of these devices are connected to ground, the unity gain buffer between Y node and X node is done through the bulks of input transistors.

The minimum supply voltage of a conventional gate driven miller op amp operating in strong inversion as expressed in equation 5 is limited by the input stage.

$$V_{(\min)} = |V_T| + 3|V_{DSsat}| \qquad (5)$$

The operation of the bulk driven MOSFET is depletion type, transistor is turned on by setting sufficient value of gate source voltage, and to modulate the current flow input voltage is applied to the bulk terminal of the transistor.

By such way of biasing, threshold limit is removed.

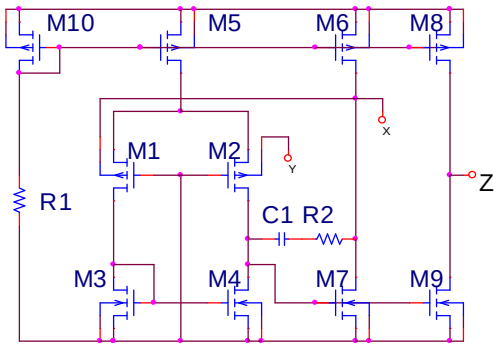


Figure 7. CCII based miller compensated bulk-driven

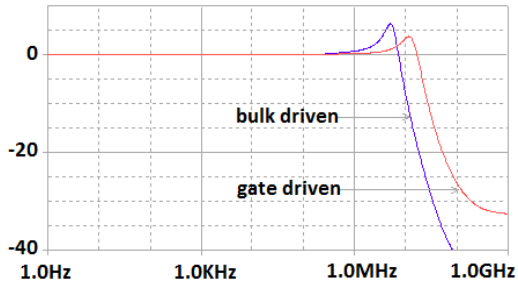


Figure 8. Current transfer between x and z nodes, iz/ix

The impedance of the Y terminal is the bulk impedance of MOS transistor which ensuring high input impedance for the voltage buffer.

$$r_y = \frac{1}{g_{mb}} = \frac{1}{g_m}\left(\frac{2\sqrt{2\phi_F - V_{BS}}}{\gamma}\right). \quad (6)$$

$$r_x \approx \frac{2}{g_{mb1} r_o (g_{m6} + g_{m7})} \quad (7)$$

$$r_z \approx \frac{r_{o8} r_{o9}}{r_{o8} + r_{oM9}} \quad (8)$$

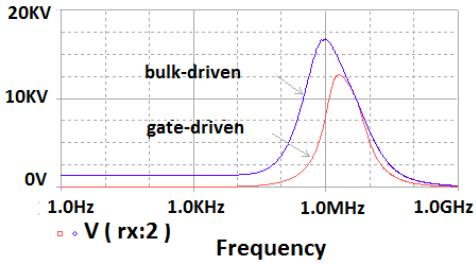


Figure 9. Impedance at x node, rx.

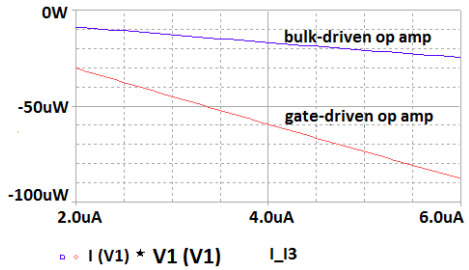


Figure 10. power dissipation of current conveyor voltage source

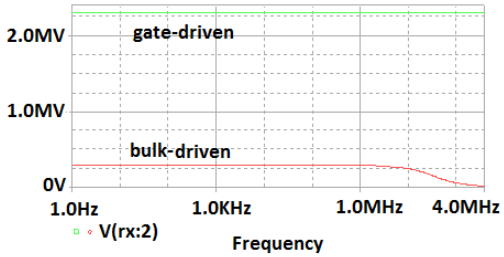


Figure 11. Output impedance at z node, rz

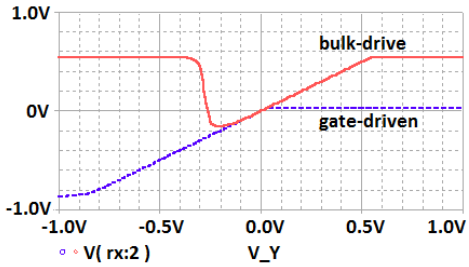


Figure 12. Voltage followers between X node and Y node

This CCII was designed to operate with a low supply voltage and reduced power dissipation, these requirement are confirmed in table 1 and foregoing simulations shown in figures 9 -12, the main advantages were verified bigger dynamic range due to the depletion characteristic allows zero, negative, and even small positive values of bias voltage to achieve the desired dc current. This can lead to larger input common mode voltage range, voltage swing that could not otherwise be achieved at low power supply voltages.

Table1. Comparison of conventional, self cascode and bulk driven Characteristics

Characteristics	LV Bulk-driven CCII	LV Gate-driven CCII	Composite Transistor CCII
Voltage Supply	± 0.6 V	±1.5 V	± 2 V
Power Consumption	16µW	70µW	80µW
3dB Bandwidth	22 MHz	13 MHz	15 MHz
Dynamic Range	-130 mV, +600 mV	-750mV, +20 mV	-1.5V, +20 mV
Node X Parasitic Resistance	15 KΩ	12k Ω	6kΩ
Node Z Parasitic Resistance	300 KΩ	2.3 MΩ	1.1 MΩ

CONCLUSION

This work focused on developing analog circuit techniques that are compatible with future CMOS technologies. One of these techniques called self-cascode does not require high compliance voltages at output nodes, it provides high output impedance to give high output gain and so it is useful in low-voltage design. The bulk driven is other technique removes the threshold voltage requirements and the device can be operated at low supply voltages. Finally, we want to remark that, for LV applications, the current-mode approach can be a valid alternative to traditional circuits to obtain high performance architectures.

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